武汉芯源半导体有限公司
WUHAN XINYUAN SEMICONDUCTOR CO., LTD

CW32L012 Datasheet

ARM® Cortex®-M0+ 32-bit low power MCU with up to 64KB FLASH, 8KB RAM

Rev 1.0

January 2026

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Contents

1 Features

- Core: ARM® Cortex®-M0+
  - Frequency up to 96MHz
- Operating temperature: -40°C~+85°C; Operating voltage: 1.7V~5.5V
- Memories
  - Maximum 64KB FLASH, data retention for 25 years @ -40°C~+85°C, support erase protection, read protection and safe runtime protection, support ISP, ICP, IAP, and 4-level security protection, support caching and prefetching.
  - Up to 8KB RAM, support hardware parity
  - 22 bytes OTP memory
- CRC calculation unit
- CORDIC coprocessor for fast trigonometric function calculation
- EAU Extended Arithmetic Unit, support division and square root
- Reset and power management
  - Low power modes (Sleep, DeepSleep)
  - Power-on/ Brown-out reset (POR/BOR)
  - Programmable low voltage detector (LVD)
- Clock management
  - 4MHz~32MHz crystal oscillator
  - 32kHz low speed crystal oscillator
  - Internal 96MHz RC oscillator
  - Internal 32kHz RC oscillator
  - Internal 10kHz RC oscillator
  - Clock monitoring system
  - Allow independent shutdown of each peripheral clock
- Up to 40 I/O ports
  - All I/O ports support filtered interrupt function
  - All I/O ports support filtered wake-up function
  - All I/O ports support hysteresis and pull-up input
  - All I/O ports support push-pull and open-drain output
- 4-channel DMA controller
- 2 12-bit analog to digital converters
  - Up to 1M SPS conversion speed, sample time for each sequence channel can be configured independently
  - 8 conversion result registers
  - Built-in 1.2V voltage reference
  - Analog watchdog function
  - Built-in temperature sensor
- 2 12-bit digital to analog converters
  - Up to 1M SPS conversion speed
  - 2 independent output channels
- 4 voltage comparators, built-in programmable reference voltage
- 2 operational amplifiers
- Real time clock and calendar
  - Support wakeup from Sleep/DeepSleep mode
- Timers

  - 1 16-bit advanced-control timer, support 6-input capture, support 6 pairs of complementary PWM outputs with dead-time, support dual point compare, and support PWM phase shift.
  - 4 16-bit general-purpose timers, support 4 channels PWM output or input capture, support multiple code counting.
  - 3 16-bit basic timers.
  - 1 16-bit low-power timer, support PWM output, support code counting, support low-power wake-up.
  - 1 24-bit Hall sensor specific timer.
  - Window watchdog timer with PCLK counting.
  - Independent watchdog timer with dedicated clock counting.
- Communication interfaces
  - 3 low-power UARTs, support asynchronous mode, synchronous mode, support fractional baud rate, support low-power receive data, support configurable level shifting, support LIN communication interface.
  - 3 SPI interfaces 24Mbit/s, support 4~16 bit width
  - 2 I2C interfaces 1Mbit/s, supports configurable level shifting, supports SMBUS
  - IR modulator, programmable duty cycle and polarity
- Serial wire debug (SWD)
- 80-bit unique ID

Table 1-1 Package model list

Series	Model	Package
CW32L012x8	CW32L012C8	LQFP48
		QFN48

2 Introduction

This datasheet provides the ordering information and electromechanical characteristics of the CW32L012 microcontrollers.

This document should be read in conjunction with the CW32L012 reference manual.

For information on the ARM® Cortex®-M0+, please refer to the *Cortex®-M0+ Technical Reference Manual* at http://www.arm.com

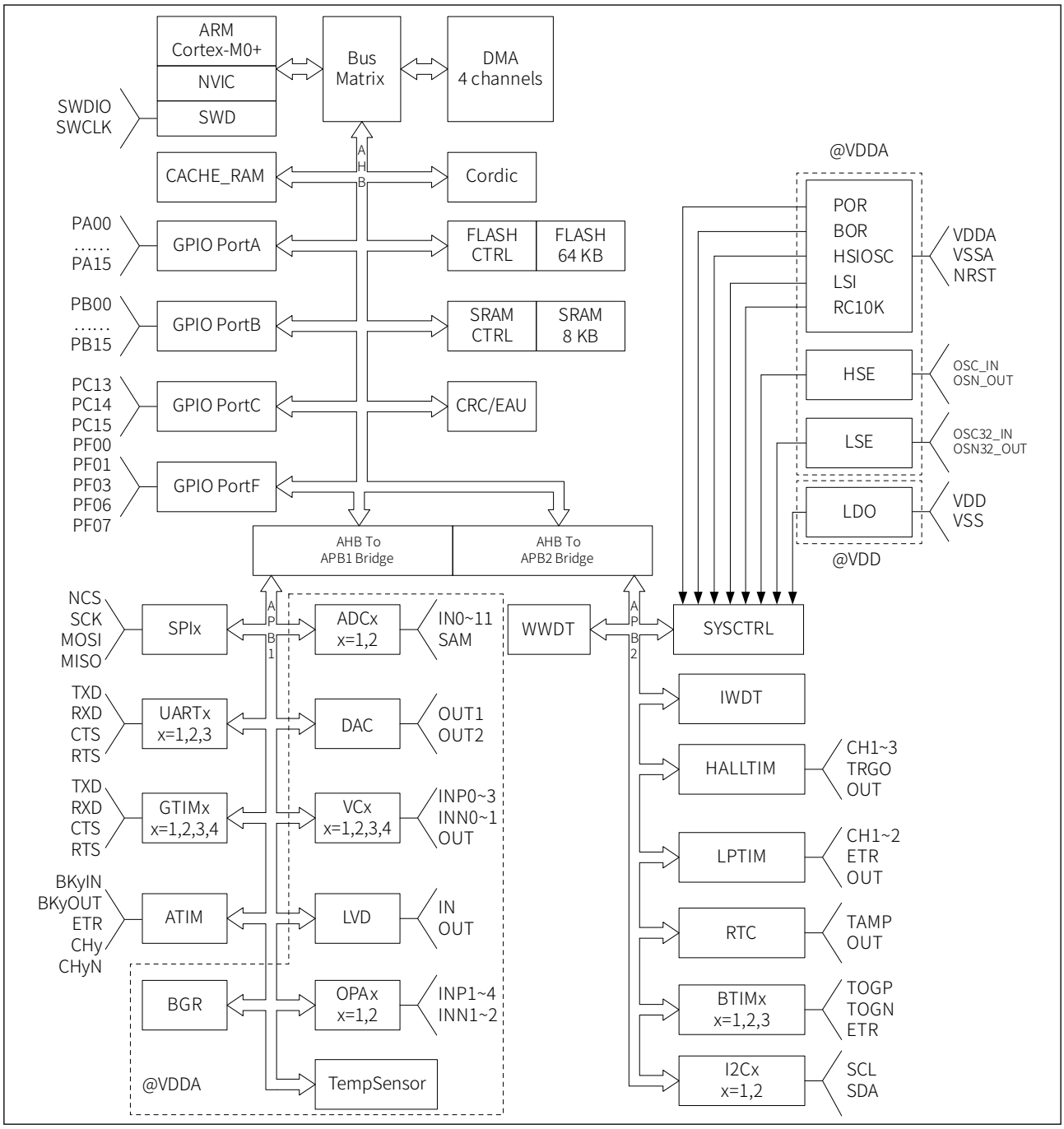
3 Description

CW32L012 is an eFlash-based single-chip Low-Power microcontroller that integrates an ARM® Cortex®-M0+ core with a main frequency up to 96MHz, high-speed embedded memories (up to 64KB bytes of FLASH and up to 8KB SRAM), and an extensive range of enhanced peripherals and I/Os.

All devices offer standard communication interfaces (3 UARTs、3 SPIs, and 2 I2Cs), 2 12-bit high speed ADCs , 2-channel 12-bit DACs, dual-channel rail-to-rail operational amplifier, 7 general-purpose and basic timers, 1 low-power timer, 1 hall sensor specific timer and 1 advanced-control PWM timer.

CW32L012 operates in the -40°C~+85°C temperature range from a 1.7V~5.5Vpower supply, supports two low-power operating modes (Sleep and DeepSleep). The internal block diagram is shown in the following figure:

Figure 3-1 Internal block diagram



CW32L012 provides 2 different packages: LQFP48, QFN48. The functions that can be achieved by products in different packages are different. The details are shown in the following table:

Table 3-1 CW32L012 family device features list

Peripheral		CW32L012C8T6	CW32L012C8U6
FLASH		64KB	
SRAM		8KB	
Timers	Advanced control	1	
	General purpose	4	
	Low power	1	
	Hall sensor specific	1	
	Basic	3	
SPI		3	
I2C		2	
UART		3	
12-bit ADC (number of input channels)		2 (12 ext. + 4 int.)	
12-bit DAC (number of output channels)		2 (2)	
GPIO		40	
Kernel frequency		96MHz	
Operating voltage		1.7V~5.5V	
Operating temperature		-40°C~+85°C	
Package		LQFP48	QFN48

4 Functional overview

4.1 ARM® Cortex®-M0+ core with embedded Flash and SRAM

The ARM® Cortex®-M0+ processor is the latest generation 32-bit core for small embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0+ 32-bit RISC processor features exceptional code-efficiency, delivering the high performance expected from an Arm core in the small memory.

The CW32L012 family has an embedded ARM® core and is therefore compatible with all ARM® tools and software.

4.2 Memories

The device has the following features:

- 8KB embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for high reliability critical applications.
- The non-volatile memory is divided into two arrays:
  - 64KB embedded Flash memory for programs and data.
  - 2KB boot program memory.
- FLASH memory erasing and reading protection: The FLASH memory erasing and writing protection is performed through the register, and the 4-level read protection level is set through the ISP command.
  - LEVEL0
    No readout protection, the FLASH memory can be read by SWD or ISP.
  - LEVEL1
    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP or SWD interface. After the downgrade, the FLASH is in the whole chip erasing state.
  - LEVEL2
    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP interface. After the downgrade, the FLASH is in the whole chip erasing state.
  - LEVEL3
    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. Protection level downgrade in any way is not supported.
- Internal 1KB instruction cache, supports Flash acceleration unit to execute program with 0 wait.

4.3 Boot mode

The CW32L012 supports the following 2 different Boot Modes, which can be selected by the BOOT pin status, as shown in the following table:

Table 4-1 Boot Mode Configuration

Boot Mode Configuration	Boot Mode
BOOT = 0	Boot from the main FLASH memory and run the user program.
BOOT = 1	Boot from the BootLoader memory and run the chip's BootLoader program fixedly, at which time the user can utilize the ISP communication protocol to program FLASH through the UART1 interface (PA13/PA14).

After the system boot is complete, the CPU fetches the address of the top of the stack from address 0x0000 0000 in memory and starts executing code from the address indicated by 0x0000 0004 in memory.

The BootLoader program is in the BootLoader memory area and is programmed by the device provider during manufacturing. The user can utilize the ISP communication protocol for FALSH programming via UART1 (pin PA13/PA14).

4.4 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit can generate the CRC code of the data stream according to the selected algorithm and parameter configuration.

In some applications, CRC techniques can be utilized to verify the integrity of data transmission and storage.

The product supports 8 commonly used CRC algorithms, including:

- CRC16_IBM
- CRC16_MAXIM
- CRC16_USB
- CRC16_MODBUS
- CRC16_CCITT
- CRC16_CCITT_FALSE
- CRC16_X25
- CRC16_XMODEM

4.5 Coordinate rotation digital computer algorithm (CORDIC)

Provides hardware acceleration for certain mathematical functions, especially trigonometric functions, which are typically used in motor control, metrology, signal processing, and many other applications. Compared with software implementation, it speeds up the calculation of these functions, allows for lower operating frequencies, or frees up processor cycles to perform other tasks.

The product supports cosine (cos), sine (sin), phase angle (atan2), modulus (hypot), arctangent (atan), hyperbolic cosine (cosh), hyperbolic sine (sinh), and hyperbolic arctangent (atanh) function operations. In idle state or after the operation is completed, DMA can be triggered for quick access.

4.6 Power management

4.6.1 Power supply schemes

- V_{DD} = 1.7V~5.5V
  Power supply for the I/O ports and internal regulator. Provided externally through VDD pins.
- V_{DDA} = 1.7V~5.5V
  Power supply for the ADC, reset circuitry, and on-chip RC oscillator. Provided externally through VDDA pins, and the V_{DDA} voltage value must be always greater or equal to the V_{DD} voltage value.

For details about the power supply, refer to Figure 7-3: Power system.

4.6.2 Power supply monitoring

The device integrates power-on reset (POR) and brown-out reset (BOR) power monitoring circuits internally, and the power supply is always in an operational state after power-on.The POR/BOR monitors the VDD and VDDA power supply voltage, and the system enters a reset state when the power supply voltage is monitored to be lower than the reset threshold ($V_{POR/BOR}$). Users do not need to add additional external hardware reset circuit.

4.6.3 Voltage regulator

The internal voltage regulator has "Normal" and "Low-power" operating modes, and it always enabled after reset.

- “Normal” mode: corresponding to the state of full- speed operation.
- “Low-power” mode: corresponding to partially powered operation, including Sleep and DeepSleep operating modes.

4.6.4 Low-power modes

The CW32L012 microcontrollers support 2 low-power modes:

- Sleep mode
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- DeepSleep mode
  DeepSleep is used to achieve the lowest power consumption, the CPU stops running, the high-speed clock modules (HSE, HSIOSC) are automatically turned off, and the low-speed clocks (LSE, LSI) remain unchanged.
  The device exits DeepSleep mode when an external reset, or an IWDT reset, or some peripheral interrupts, or an RTC event occurs.

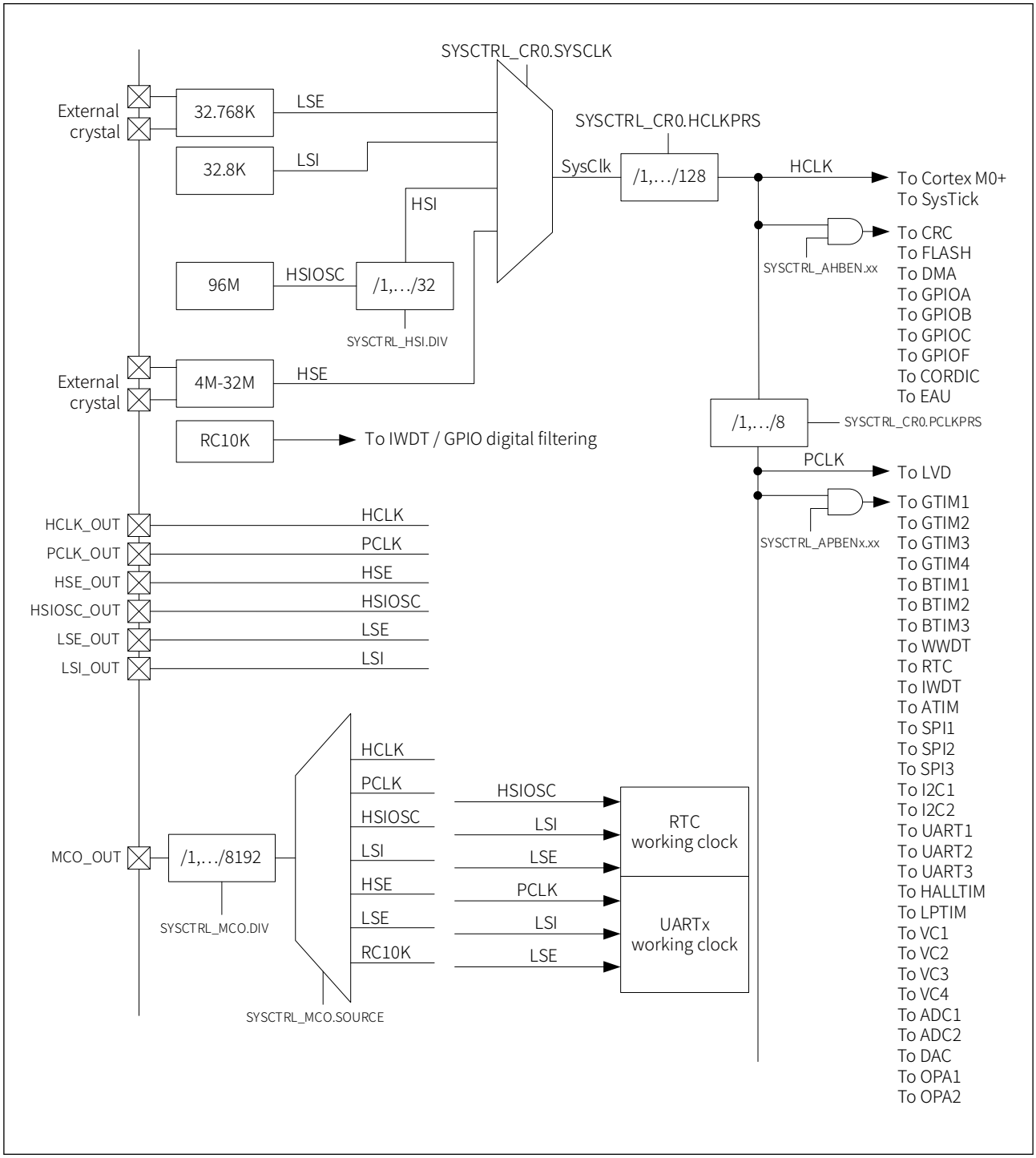
4.7 Clocks and startup

After the MCU is reset, the HSI (generated by the internal 96MHz HSIOSC oscillator frequency division) is selected as the clock source of SysClk by default, and the default value of the system clock frequency is 4MHz.The user can use the program to start the external crystal oscillator and switch the system clock source to the external clock source. The clock failure detection module can continuously detect the state of the external clock source. Once the failure of the external clock source is detected, the system will automatically switch to the internal HSIOSC clock source. If the corresponding fault detection interrupt is enabled, an interrupt will be generated for the user to record fault events.

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 96MHz.

The internal clock tree of the system is shown below :

Figure 4-1 Clock tree of CW32L012



4.8 General-purpose inputs/outputs (GPIO)

Each GPIO pin can be software configured as a push-pull or open-drain digital output, or as a digital input with internal pull-up or pull-down, as well as peripheral multiplexing.Some GPIO pins have analog functionality and interface with internal analog peripherals.All I/Os can be configured as external interrupt input pins with digital filtering.

4.9 Direct memory access controller (DMA)

The chip has a built-in DMA controller, 4 independent channels, high-speed data transmission between peripherals and memory, between peripherals and peripherals, and between memory and memory.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. The software can configure the transmission direction and data length of each channel individually.

4.10 Nested vectored interrupt controller (NVIC)

The CW32L012 family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0+) and supports programmable 4 priority levels.

- Interrupt entry vector table address can be remapped
- Closely coupled NVIC core interface
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved

This hardware block provides flexible interrupt management features with minimal interrupt latency.

4.11 Analog to digital converter (ADC)

Built-in 2 12-bit analog to digital converter with up to 12 external and 4 internal channels (DAC_OUT1/ DAC_OUT2 conversion results, temperature sensor, BGR 1.2V voltage reference), and supports sequence channel conversions mode.。

In sequence channel mode, automatic conversion is performed for a selected set of analog inputs.

The ADC can provide data to the DMA controller.

The analog watchdog function can monitor the conversion voltages of several selected channels precisely. An interrupt will be generated when the conversion voltage is within the set threshold range.

4.11.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of temperature sensor measurement, manufacturers perform individual factory calibrations for each chip. Temperature sensor factory calibration data is stored in FLASH memory.

Table 4-2 Internal temperature sensor calibration value address

ADC reference voltage	Calibration value storage address	Calibration value accuracy
V_{DDA}	0x0010 07CE - 0x0010 07CF	±3°C

4.11.2 Internal voltage reference

The nominal output voltage of the built-in BGR module of this chip is 1.2V. The voltage output by BGR module of each chip is slightly different. The voltage output by BGR module has been accurately measured at the factory and stored in FLASH. The voltage value can be read out by using the expression *((uint16_t) 0x0010 07D2)*, and its unit is mV.

4.12 Digital to analog converter (DAC)

CW32L012 integrates a 2-channel digital-to-analog converter (DAC) internally, offering 8-bit or 12-bit resolution, and is equipped with a built-in noise generator and a triangular wave generator. The digital signals of the Data Holding Register (DHR), the built-in noise generator and the triangular wave generator can be converted into analog signals. The conversion results can be output through 2 independent output channels and support both single-channel and dual-channel modes. The conversion results can also provide data for ADC, VC and OPA. Meanwhile, the DAC supports DMA transmission function, allowing for high-speed data transfer between DHR registers and memory without CPU intervention.

- 8-bit or 12-bit resolution
- Noise generator
- Triangular wave generator
- 3 input conversion channels
  - Data Holding Register (DHR)
  - Built-in noise generator
  - Triangular wave generator
- 2 independent output channels
- Supports single-channel left-aligned/right-aligned data formats and dual-channel mode in 12-bit mode
- Supports single-channel left-aligned/right-aligned data formats and dual-channel mode in 8-bit mode
- The VDDA power supply voltage serves as both the power supply and reference voltage source (Vref)
- Supports on-chip peripheral automatic triggering of DAC conversion
- Supports direct memory access (DMA)

4.13 Analog voltage comparator (VC)

It integrates 4 analog voltage comparators (VCs) internally to compare the voltages of two analog input channels and output the comparison results from the pins. The positive terminal input of the voltage comparator supports up to 4 external analog inputs, and the negative terminal supports not only 2 external analog inputs, but also internal DAC conversion result and internal resistance voltage divider output voltage. The comparison result output has filtering function, hysteresis window function, and polarity selection. Support compare interrupt, which can be used to wake up MCU in low power mode.

The main features of an analog voltage comparator (VC) are:

- Dual analog voltage comparator VC1, VC2, VC3, VC4
- Internal 8-step resistor divider
- 4 external analog signal inputs
- 2 on-chip analog input signals
  - The internal resistor divider output voltage
  - The internal DAC conversion result
- Selectable output polarity
- Support hysteresis window compare function
- Programmable filters and filter times
- 3 interrupt triggering methods, which can be used in combination
  - High level trigger
  - Rising edge trigger
  - Falling edge trigger
- Support running in low-power mode, interrupt wake-up MCU

4.14 Low voltage detector (LVD)

Low voltage detector (LVD) is used to monitor the VDDA power supply voltage or external pin input voltage. When the comparison results between the monitored voltage and the LVD threshold meets the trigger condition, an LVD interrupt or reset signal will be generated, which is usually used to handle some urgent tasks.

The interrupt and reset flags generated by the LVD can only be cleared by software; only after the interrupt or reset flag is cleared and the trigger condition is reached again, the LVD can generate an interrupt or reset signal again.

The main features of a low voltage detector (LVD) are:

- 2-channel monitoring voltage source:
  VDDA power supply voltage, PA00 pin input.
- 8-step threshold voltage, range 1.8V~4.6V
- 3 trigger conditions, which can be used in combination
  - Level Triggered: voltage below threshold
  - Falling edge trigger: the falling edge when the voltage falls below the threshold
  - Rising edge trigger: the rising edge when the voltage rises back above the threshold
- Can trigger to generate interrupt or reset signal, but both cannot be generated at the same time
- Programmable filter and filter time
- Support hysteresis function
- Support running in low-power mode, interrupt wake-up MCU

4.15 Operational amplifier (OPA)

CW32L012 integrates 2 operational amplifiers (OPAs) internally, which, when combined with external circuitry, can perform various functions of a general-purpose op-amp. The positive input of the OPA supports up to three external analog inputs and one internal DAC, while the negative input supports 2 external analog inputs. OPA has a calibration function and can be triggered to start OPA calibration in multiple ways.

4.16 Extended arithmetic unit (EAU)

The extended arithmetic unit (EAU) is a coprocessor specifically designed for arithmetic operations, supporting efficient execution of signed integer division, unsigned integer division, and unsigned integer square root operations to obtain quotients/square roots and remainders. It is an effective supplement and extension to the arithmetic instructions of the M0+ core. It has the following characteristics:

- Supports 32-bit division by 32-bit signed/unsigned integer division operations to obtain the quotient and remainder.
- Supports 32-bit unsigned integer square root operations to obtain square root and remainder.
- Unsigned division supports the zero divisor flag.
- Signed division supports the zero divisor flag and the overflow flag.

4.17 Timers, counters and watchdogs

The CW32L012 microcontroller integrates up to 4 general-purpose timers, 3 basic timers, 1 low-power timer, 1 advanced control timer and 1 Hall sensor specialized timer.

The function differences of timers are shown in the following table:

Table 4-3 Timer feature comparison

Timer type	Timer/ Counter	Counter bit width	Counter type	Prescaler factor	DMA request	Capture/ compare channels	Complementary outputs
Advanced control	ATIM	16-bit	Up, down, up/down	1,2,3,4, …,65536	YES	6	6
General purpose	GTIM	16-bit	Up, down, up/down	1,2,3,4, …,65536	YES	4	0
Low-power	LPTIM	16-bit	Up, down, up/down	2^N (N=0,..7)	YES	2	0
Basic	BTIM1	16-bit	Up	1,2,3,4, …,65536	YES	0	1
	BTIM2	16-bit	Up	1,2,3,4, …,65536	YES	0	1
	BTIM3	16-bit	Up	1,2,3,4, …,65536	YES	0	1
Hall sensor specialized	HALLTIM	16-bit	Up	1,2,4,8	YES	3	0

4.17.1 Advanced-control timer (ATIM)

The Advanced-control Timer (ATIM) consists of a 16-bit auto-reload counter, driven by a programmable prescaler. ATIM supports timing, counting, reset, gating, trigger and encoder modes, with 6 independent capture/compare channels, enabling 6 independent PWM outputs or 6 pairs of complementary PWM outputs with dead zones or capture of 6 inputs. Can be used for basic timing/counting, measuring pulse width and period of input signals, generating output waveforms (PWM, single pulse, complementary PWM with dead time inserted, etc.). In addition, ATIM supports DMA requests.

4.17.2 General-purpose timer (GTIM1..4)

The CW32L012 integrates 4 general-purpose timers (GTIMs), each of which is completely independent and functionally identical, and each of which consists of a 16-bit auto-reload counter driven by a programmable prescaler. GTIMs support Timing, Counting, Reset, Gating, Trigger and Encoder modes of operation. GTIM supports Timing, Counting, Reset, Gating, Trigger and Encoder modes of operation. Each GTIM has 4 independent capture/compare channels, which can measure the pulse width of the input signals (Input Capture) or generate output waveforms (Output Compare and PWM). In addition, GTIM also supports DMA requests.

4.17.3 Low-power timer (LPTIM)

The internal integration of a 16-bit low power timer (LPTIM) can realize the function of timing or counting external pulses with very low power consumption. By selecting a suitable clock source and trigger signal, it can realize the function of waking up the system when it sleeps with low power consumption. LPTIM has an internal comparison register, which can realize the comparison output and PWM output, and can control the polarity of the output waveform. In addition, LPTIM can be connected with a quadrature encoder to automatically realize counting up and down.

4.17.4 Basic timers (BTIM1..3)

Three basic timers (BTIMs) are integrated internally, each completely independent and functionally identical, each containing a 16-bit automatic reload counter and driven by a programmable prescaler.BTIM supports four working modes: internal counting mode, external counting mode, trigger startup mode and gated counting mode. It supports interrupt when update event and trigger event occur.Counter reset can be controlled by reset input signal under different working modes.

4.17.5 Hall sensor dedicated timer (HALLTIM)

CW32L012 integrates 1 24-bit up-counter Hall sensor-specific timer (HALLTIM) internally. It is a circuit integrated with a Hall effect sensor, used to detect magnetic fields and convert them into electrical signals. It is commonly used in applications such as motor control and position detection. It has 3 independent capture channels and 1 output, capable of outperforming PWM, output comparison, HALL signal variation pulses, and 3-channel filtered signal XOR, etc. In addition, HALLTIM also supports DMA requests.

4.17.6 Independent watchdog (IWDT)

The CW32L012 integrates an independent watchdog timer (IWDT) that uses a dedicated internal RC clock source, RC10K, to avoid external influences during operation.. once the IWDT is started, the user needs to reload the counter of the IWDT within a specified time interval, otherwise an overflow will trigger a reset or generate an interrupt signal. After the IWDT is started, the counting can be stopped. The user can choose to keep the IWDT running or suspend counting while in DeepSleep mode.

A specially set key-value register can lock the key registers of the IWDT to prevent the registers from being accidentally modified.

4.17.7 System window watchdog (WWDT)

CW32L012 integrates a window watchdog timer (WWDT), the user needs to refresh within the set time window, otherwise the watchdog overflow will trigger a system reset. WWDT is usually used to monitor the program execution flow with strict time requirements to prevent the abnormal execution of the application program caused by external interference or unknown conditions, resulting in system failure.

4.17.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features are:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.

4.18 Real-time clock (RTC)

The Real Time Clock (RTC) is a dedicated counter/timer that provides calendar information including hours, minutes, seconds, subseconds, date, month, year, and week day.

RTC has two independent alarm clocks, the time and date can be set in combination, and the alarm clock interrupt can be generated and output through the pin; it supports the time stamp function, which can be triggered by the pin, record the current date and time, and generate a time stamp interrupt at the same time; Support periodic interrupt; support automatic wake-up function, which can generate interrupts and output through pins; support 1Hz square wave and RTCOUT output functions; support internal clock calibration compensation.

The CW32L012 has internal independently calibrated RC clock source with a frequency of 32kHz to provide the drive clock for the RTC. The RTC can run in DeepSleep mode and is suitable for applications requiring low power consumption.

4.19 Inter-integrated circuit interfaces (I2C)

The CW32L012 integrates 2 internal I2C controllers, which can serially transmit data to the I2C bus according to the I2C specification at the set transmission rate, and at the same time detect the status during the communication process, and support bus conflict and arbitration processing for multi-master communication.

The main features of the I2C controllers are the following:

- Support master transmit/receive and slave transmit/receive four operating modes
- Support clock stretching (clock synchronization) and multi-master communication conflict arbitration
- Support standard (100Kbps) / fast (400Kbps) / fast + (1Mbps) 3 operating rates
- Support for Fast+(1Mbps) mode in slave mode
- Support 7bit/10bit addressing function
- Support 3 slave addresses
- Support broadcast address
- Support input signal noise filtering function
- Support interrupt status query function
- Support SMBUS timeout detection
- Support communication with devices operating at lower voltages than the MCU (via VC)

4.20 Universal asynchronous receiver/transmitter (UART)

The CW32L012 integrates 3 universal asynchronous receivers/transmitters (UARTs) internally, which support asynchronous full-duplex, synchronous half-duplex and single-wire half-duplex modes, support hardware data flow control and multi-machine communication, also support LIN (Local Interconnect Network). The data frame structure is programmable, and a wide range of baud rate selection can be provided through the fractional baud rate generator. Built-in timer module supports wait timeout detection, receive idle detection, automatic baud rate detection and general timing functions.

The UART controller works in a dual clock domain, allowing data reception in DeepSleep mode, and the reception completion interrupt can wake the MCU back to Active mode.

4.21 Serial peripheral interface (SPI)

The CW32L012 integrates 3Serial Peripheral Interfaces (SPIs), supporting bidirectional full-duplex, single-line half-duplex and simplex communication modes. It can be configured with an MCU as the master or slave, and supports multi-master communication mode.

The main features of the serial peripheral interfaces (SPIs) are the following:

- Support master mode, slave mode
- Support full-duplex, single-wire half-duplex, simplex
- 4-bit to 16-bit selectable data frame width
- Support transmitting/receiving data LSB or MSB first
- Clock polarity and clock phase is programmable
- SCK frequency up to 24MHz in master mode
- Support multi-machine communication mode
- 8 interrupt sources with flag bits
- Support inter-frame interval adjustment in master mode
- Support direct memory access (DMA)

4.22 Infrared modulation transmitter (IR)

Internal integrated infrared modulation transmitter (IR), through the timer, UART and IRSW soft control bits with the use of a variety of standard PWM or PPM coding can be easily achieved, can also achieve UART data infrared modulation transmission.

The main characteristics of the infrared modulation transmitter (IR) are the following:

- SIR that supports IrDA standard 1.0
- Maximum data rate of 115.2kbps
- IR emitter tube adaptable to high and low levels

4.23 Serial wire debug port (SWD)

An ARM® SWD interface is provided, and users can use the CW-DAPLINK of Xinyuan Semiconductor to connect to the MCU to debug and simulate in the IDE development environment.

5 Pin descriptions

Figure 5-1 LQFP48 package pinout (top view)

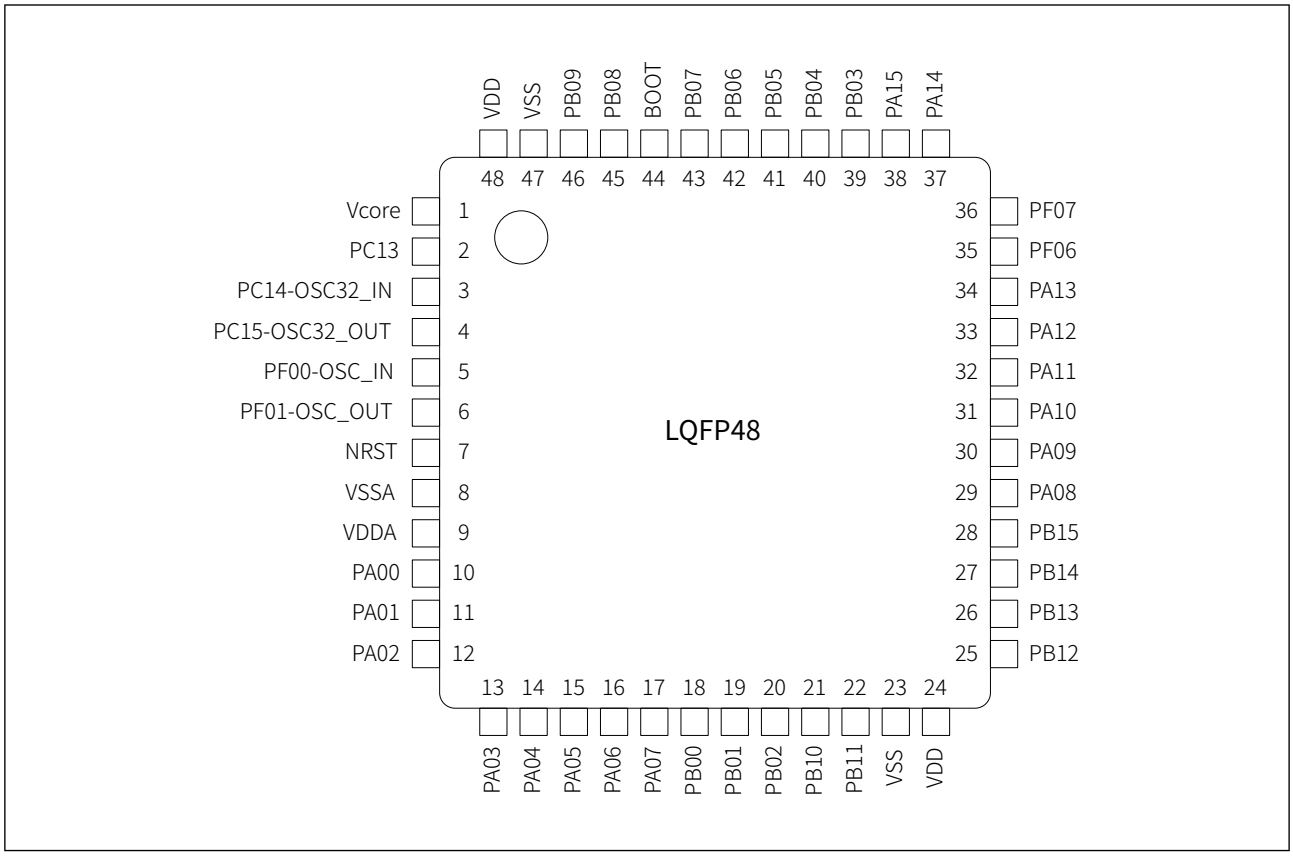


Figure 5-2 QFN48 package pinout (top view)

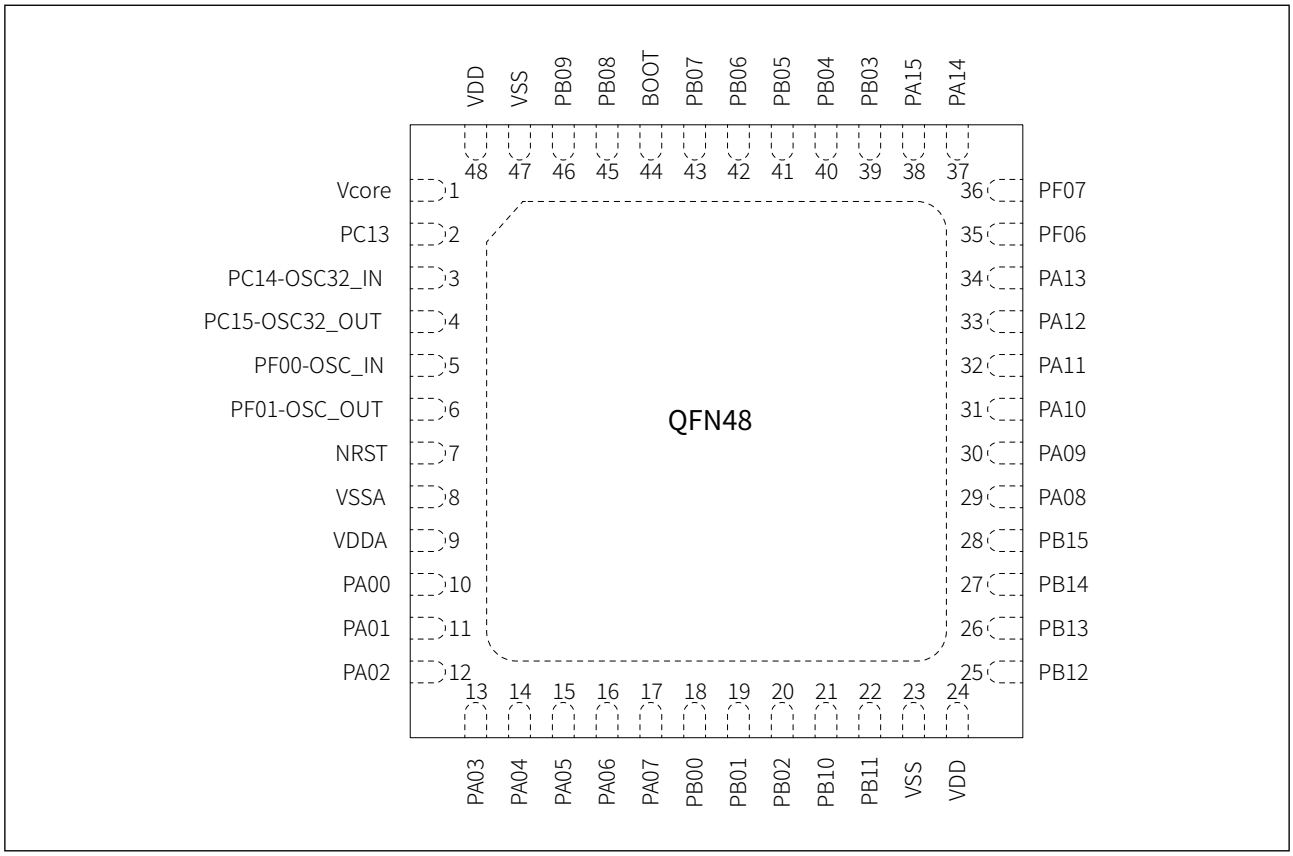


Table 5-1 Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function after reset is the same as the actual pin name.	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/output pin
I/O structure	TTa	Connect the I/O port for the analog function
	TC	Standard I/ O pin
	B	Dedicated BOOT pin
	RST	Reset input pin
Notes	Unless otherwise specified by a note, all pins are set as high impedance input state after reset.	
Additional functions	Digital function	Functions selected through GPIOx_AFRy registers
	Analog function	Functions directly selected through peripheral registers

Table 5-2 CW32L012 pin definitions

Pin No.		Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
LQFP48	QFN48					Digital function	Analog function
1	1	Vcore	-	-	-	Vcore is the regulator supply output, must be connected to 4.7μF capacitor to ground, and only for internal circuit use	
2	2	PC13	I/O	TC	-	MCO_OUT, RTC_TAMP, RTC_OUT, BTIM2_ETR, ATIM_BK, ATIM_ETR, GTIM3_ETR, GTIM4_ETR	
3	3	PC14	I/O	TC	-	UART1_RXD, UART2_RXD, UART3_CTS, I2C1_SDA, BTIM2_TOGN, ATIM_CH6, ATIM_CH5N, SPI3_MISO, GTIM4_CH1	OSC32_IN
4	4	PC15	I/O	TC	-	UART1_TXD, UART2_TXD, UART3_RTS, I2C1_SCL, BTIM2_TOGP, ATIM_CH6N, ATIM_CH5, SPI3_MOSI, GTIM4_CH2	OSC32_OUT
5	5	PF00	I/O	TC	-	UART1_RXD, I2C1_SDA, BTIM1_TOGN, GTIM1_TRGO, ATIM_CH6N, SPI3_SCK, GTIM4_CH3	OSC_IN
6	6	PF01	I/O	TC	-	UART1_TXD, HEXEN, LSE_OUT, I2C1_SCL, BTIM1_TOGP, GTIM2_TRGO, ATIM_CH6, SPI3_CS, GTIM4_CH4	OSC_OUT
7	7	NRST	I	RST	-	Device reset input	
8	8	VSSA	S	-	-	Analog ground	
9	9	VDDA	S	-	-	Analog power supply	
10	10	PA00	I/O	TTa	-	UART1_CTS, UART3_RXD, RTC_TAMP, VC1_OUT, BTIM3_TOGN, GTIM2_CH1, ATIM_BK, SPI2_MISO, VC3_OUT	ADC1_IN0, VC1_CH0, LVD_IN
11	11	PA01	I/O	TTa	-	UART1_RTS, UART3_TXD, RTC_OUT, HEXEN, BTIM3_TOGP, GTIM2_CH2, ATIM_ETR, SPI2_MOSI	ADC1_IN1, VC2_CH0
12	12	PA02	I/O	TTa	-	UART1_TXD, UART2_TXD, BTIM2_ETR, VC2_OUT, LPTIM_CH1, GTIM2_CH3, ATIM_CH4N, SPI2_SCK	ADC1_IN2, VC1_CH1
13	13	PA03	I/O	TTa	-	UART1_RXD, UART2_RXD, RTC_OUT, PCLK_OUT, LPTIM_CH2, GTIM2_CH4, ATIM_CH4, SPI2_CS, HALLTIM_CH1	ADC1_IN3, VC2_CH1, OPA1_INP1
14	14	PA04	I/O	TTa	-	UART3_TXD, I2C1_SCL, SPI1_CS, MCO_OUT, LPTIM_OUT, ADC2_SAM, ATIM_CH2N, GTIM3_CH1, HALLTIM_CH2	ADC1_IN4, VC1_CH2, OPA1_INN1, OPA2_INP1

Table 5-2 CW32L012 pin definitions (continued)

Pin No.		Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
LQFP48	QFN48					Digital function	Analog function
15	15	PA05	I/O	TTa	-	UART3_RXD, I2C1_SDA, SPI1_SCK, BTIM2_TOGN, LPTIM_ETR, GTIM1_CH3, ATIM_CH1, GTIM3_CH2, HALLTIM_CH3	ADC1_IN5, ADC2_IN0, VC2_CH2, OPA2_INN1
16	16	PA06	I/O	TTa	-	UART2_RXD, BTIM1_ETR, SPI1_MISO, BTIM2_TOGP, LPTIM_CH1, GTIM1_CH1, ATIM_BK, GTIM3_CH3	ADC1_IN6, ADC2_IN1, VC3_CH0, OPA1_INP2, OPA2_INP2
17	17	PA07	I/O	TTa	-	UART2_TXD, GTIM2_ETR, SPI1_MOSI, BTIM1_TOGN, LPTIM_CH2, GTIM1_CH2, ATIM_CH1N, GTIM3_CH4	ADC1_IN7, ADC2_IN2, VC3_CH1, OPA1_INN2, OPA2_INN2
18	18	PB00	I/O	TTa	-	UART1_RXD, UART2_TXD, HSIOSC_OUT, BTIM1_TOGP, ATIM_ETR, GTIM1_CH3, ATIM_CH2N, I2C2_SCL, HALLTIM_OUT	ADC1_IN8, ADC2_IN3, VC1_CH3, VC3_CH3, DAC_OUT1, OPA1_OUT, OPA2_INP3
19	19	PB01	I/O	TTa	-	UART1_TXD, UART2_RXD, RTC_TAMP, IR_OUT, BTIM3_TOGN, GTIM1_CH4, ATIM_CH3N, I2C2_SDA, HALLTIM_TRGO	ADC1_IN9, ADC2_IN4, VC2_CH3, VC4_CH3, DAC_OUT2, OPA1_INP3, OPA2_OUT
20	20	PB02	I/O	TTa	-	UART3_TXD, UART2_CTS, ATIM_BKOUT, HSE_OUT, BTIM3_TOGP, GTIM1_ETR, ATIM_CH1, GTIM3_TRGO, HALLTIM_CH1	ADC1_IN11, ADC2_IN11, VC3_CH2
21	21	PB10	I/O	TTa	-	UART3_RXD, UART2_RTS, I2C1_SCL, ATIM_BK2, VC4_OUT, GTIM2_CH3, ATIM_CH2, I2C2_SCL, HALLTIM_CH2	ADC1_IN10, ADC2_IN10, VC4_CH2
22	22	PB11	I/O	TC	-	UART1_RXD, ATIM_BK2OUT, I2C1_SDA, LSI_OUT, BTIM1_ETR, GTIM2_CH4, ATIM_CH3, I2C2_SDA, HALLTIM_CH3	
23	23	VSS	S	-	-	Digital ground	
24	24	VDD	S	-	-	Digital power supply	

Table 5-2 CW32L012 pin definitions (continued)

Pin No.		Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
LQFP48	QFN48					Digital function	Analog function
25	25	PB12	I/O	TC	-	UART1_TXD, LPTIM_OUT, SPI1_CS, LSE_OUT, VC1_OUT, ATIM_TRGO, ATIM_BK, SPI2_CS, HALLTIM_OUT	
26	26	PB13	I/O	TC	-	UART2_RXD, LPTIM_ETR, SPI1_SCK, ATIM_BK2, VC2_OUT, ATIM_TRGO2, ATIM_CH1N, SPI2_SCK, HALLTIM_CH1	
27	27	PB14	I/O	TC	-	UART2_TXD, LPTIM_CH2, SPI1_MISO, RTC_OUT, VC3_OUT, GTIM2_CH1, ATIM_CH2N, SPI2_MISO, HALLTIM_CH2	
28	28	PB15	I/O	TC	-	UART3_RXD, LPTIM_CH1, SPI1_MOSI, RTC_OUT, BTIM2_TOGN, GTIM2_CH2, ATIM_CH3N, SPI2_MOSI, HALLTIM_CH3	
29	29	PA08	I/O	TTa	-	UART3_TXD, VC4_OUT, IR_OUT, MCO_OUT, BTIM2_TOGP, LVD_OUT, ATIM_CH1, SPI3_CS, GTIM4_ETR	ADC2_IN5
30	30	PA09	I/O	TTa	-	UART1_TXD, UART3_RXD, SPI1_CS, I2C1_SCL, LPTIM_ETR, BTIM1_TOGN, ATIM_CH2, SPI3_SCK, GTIM4_CH1	ADC2_IN6, VC4_CH0
31	31	PA10	I/O	TTa	-	UART1_RXD, BTIM3_ETR, SPI1_SCK, I2C1_SDA, LPTIM_OUT, BTIM1_TOGP, ATIM_CH3, SPI3_MISO, GTIM4_CH2	ADC2_IN7, VC4_CH1
32	32	PA11	I/O	TTa	-	UART1_CTS, VC1_OUT, SPI1_MISO, HEXEN, ATIM_BK2, GTIM2_CH2, ATIM_CH4, SPI3_MOSI, GTIM4_CH3	ADC2_IN8
33	33	PA12	I/O	TTa	-	UART1_RTS, VC2_OUT, SPI1_MOSI, BTIM3_ETR, ATIM_BK, GTIM2_CH3, ATIM_ETR, GTIM3_ETR, GTIM4_CH4	ADC2_IN9
34	34	PA13/ SWDIO	I/O	TC	1	UART1_RXD, UART3_TXD, UART2_RTS, I2C1_SDA, ATIM_BK, IR_OUT, ATIM_CH6, ATIM_CH5N	
35	35	PF06	I/O	TC	-	UART1_CTS, UART3_RXD, UART2_CTS, I2C1_SCL, BTIM3_TOGN, GTIM2_TRGO, ATIM_CH5, I2C2_SCL, GTIM4_TRGO	
36	36	PF07	I/O	TC	-	UART1_RTS, UART3_TXD, UART2_RTS, I2C1_SDA, BTIM3_TOGP, GTIM1_TRGO, ATIM_CH5N, I2C2_SDA, SPI2_CS	

Table 5-2 CW32L012 pin definitions (continued)

Pin No.		Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
LQFP48	QFN48					Digital function	Analog function
37	37	PA14/ SWCLK	I/O	TC	1	UART1_TXD, UART3_RXD, UART2_CTS, I2C1_SCL, ATIM_BK2, GTIM1_ETR, ATIM_CH6N, ATIM_CH5	
38	38	PA15	I/O	TC	-	UART1_RXD, UART2_RXD, SPI1_CS, ATIM_BKOUT, GTIM2_CH1, GTIM2_ETR, ATIM_CH1N, GTIM3_CH1, SPI2_SCK	
39	39	PB03	I/O	TC	-	UART1_TXD, UART2_TXD, SPI1_SCK, UART3_CTS, GTIM2_CH2, GTIM1_ETR, ATIM_CH2N, GTIM3_CH2, SPI2_MISO	
40	40	PB04	I/O	TC	-	UART3_TXD, UART2_CTS, SPI1_MISO, UART3_RTS, ATIM_ETR, GTIM1_CH1, ATIM_CH3N, GTIM3_CH3, SPI2_MOSI	
41	41	PB05	I/O	TC	-	UART3_RXD, UART2_RTS, SPI1_MOSI, ADC1_SAM, ATIM_BK, GTIM1_CH2, ATIM_CH1, GTIM3_CH4, HALLTIM_CH1	
42	42	PB06	I/O	TC	-	UART1_TXD, UART2_RXD, I2C1_SCL, BTIM3_TOGN, GTIM2_CH3, GTIM1_CH3, ATIM_CH2, SPI3_MOSI, HALLTIM_CH2	
43	43	PB07	I/O	TC	-	UART1_RXD, UART2_TXD, I2C1_SDA, BTIM3_TOGP, GTIM2_CH4, GTIM1_CH4, ATIM_CH3, SPI3_MISO, HALLTIM_CH3	
44	44	PF03/ BOOT	I/O	B	-	LSE_OUT, LSI_OUT, ADC1_SAM, LVD_OUT, HCLK_OUT, ATIM_TRGO, IR_OUT, GTIM3_TRGO, GTIM4_TRGO	
45	45	PB08	I/O	TC	-	UART2_RXD, UART3_TXD, I2C1_SCL, ADC2_SAM, ATIM_CH4N, GTIM1_CH3, ATIM_ETR, SPI3_SCK	
46	46	PB09	I/O	TC	-	UART2_TXD, UART3_RXD, I2C1_SDA, IR_OUT, ATIM_CH4, GTIM1_CH4, ATIM_BK, SPI3_CS	
47	47	VSS	S	-	-	Digital ground	
48	48	VDD	S	-	-	Digital power supply	

Table 5-3 Alternate functions selected through GPIOA_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PA00	UART1_CTS	UART3_RXD	RTC_TAMP	VC1_OUT	BTIM3_TOGN	GTIM2_CH1	ATIM_BK	SPI2_MISO	VC3_OUT
PA01	UART1_RTS	UART3_TXD	RTC_OUT	HEXEN	BTIM3_TOGP	GTIM2_CH2	ATIM_ETR	SPI2_MOSI	
PA02	UART1_TXD	UART2_TXD	BTIM2_ETR	VC2_OUT	LPTIM_CH1	GTIM2_CH3	ATIM_CH4N	SPI2_SCK	
PA03	UART1_RXD	UART2_RXD	RTC_OUT	PCLK_OUT	LPTIM_CH2	GTIM2_CH4	ATIM_CH4	SPI2_CS	HALLTIM_CH1
PA04	UART3_TXD	I2C1_SCL	SPI1_CS	MCO_OUT	LPTIM_OUT	ADC2_SAM	ATIM_CH2N	GTIM3_CH1	HALLTIM_CH2
PA05	UART3_RXD	I2C1_SDA	SPI1_SCK	BTIM2_TOGN	LPTIM_ETR	GTIM1_CH3	ATIM_CH1	GTIM3_CH2	HALLTIM_CH3
PA06	UART2_RXD	BTIM1_ETR	SPI1_MISO	BTIM2_TOGP	LPTIM_CH1	GTIM1_CH1	ATIM_BK	GTIM3_CH3	
PA07	UART2_TXD	GTIM2_ETR	SPI1_MOSI	BTIM1_TOGN	LPTIM_CH2	GTIM1_CH2	ATIM_CH1N	GTIM3_CH4	
PA08	UART3_TXD	VC4_OUT	IR_OUT	MCO_OUT	BTIM2_TOGP	LVD_OUT	ATIM_CH1	SPI3_CS	GTIM4_ETR
PA09	UART1_TXD	UART3_RXD	SPI1_CS	I2C1_SCL	LPTIM_ETR	BTIM1_TOGN	ATIM_CH2	SPI3_SCK	GTIM4_CH1
PA10	UART1_RXD	BTIM3_ETR	SPI1_SCK	I2C1_SDA	LPTIM_OUT	BTIM1_TOGP	ATIM_CH3	SPI3_MISO	GTIM4_CH2
PA11	UART1_CTS	VC1_OUT	SPI1_MISO	HEXEN	ATIM_BK2	GTIM2_CH2	ATIM_CH4	SPI3_MOSI	GTIM4_CH3
PA12	UART1_RTS	VC2_OUT	SPI1_MOSI	BTIM3_ETR	ATIM_BK	GTIM2_CH3	ATIM_ETR	GTIM3_ETR	GTIM4_CH4
PA13/ SWDIO	UART1_RXD	UART3_TXD	UART2_RTS	I2C1_SDA	ATIM_BK	IR_OUT	ATIM_CH6	ATIM_CH5N	
PA14/ SWCLK	UART1_TXD	UART3_RXD	UART2_CTS	I2C1_SCL	ATIM_BK2	GTIM1_ETR	ATIM_CH6N	ATIM_CH5	
PA15	UART1_RXD	UART2_RXD	SPI1_CS	ATIM_BKOUT	GTIM2_CH1	GTIM2_ETR	ATIM_CH1N	GTIM3_CH1	SPI2_SCK

Table 5-4 Alternate functions selected through GPIOB_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PB00	UART1_RXD	UART2_TXD	HSIOSC_OUT	BTIM1_TOGP	ATIM_ETR	GTIM1_CH3	ATIM_CH2N	I2C2_SCL	HALLTIM_OUT
PB01	UART1_TXD	UART2_RXD	RTC_TAMP	IR_OUT	BTIM3_TOGN	GTIM1_CH4	ATIM_CH3N	I2C2_SDA	HALLTIM_TRGO
PB02	UART3_TXD	UART2_CTS	ATIM_BKOUT	HSE_OUT	BTIM3_TOGP	GTIM1_ETR	ATIM_CH1	GTIM3_TRGO	HALLTIM_CH1
PB03	UART1_TXD	UART2_TXD	SPI1_SCK	UART3_CTS	GTIM2_CH2	GTIM1_ETR	ATIM_CH2N	GTIM3_CH2	SPI2_MISO
PB04	UART3_TXD	UART2_CTS	SPI1_MISO	UART3_RTS	ATIM_ETR	GTIM1_CH1	ATIM_CH3N	GTIM3_CH3	SPI2_MOSI
PB05	UART3_RXD	UART2_RTS	SPI1_MOSI	ADC1_SAM	ATIM_BK	GTIM1_CH2	ATIM_CH1	GTIM3_CH4	HALLTIM_CH1
PB06	UART1_TXD	UART2_RXD	I2C1_SCL	BTIM3_TOGN	GTIM2_CH3	GTIM1_CH3	ATIM_CH2	SPI3_MOSI	HALLTIM_CH2
PB07	UART1_RXD	UART2_TXD	I2C1_SDA	BTIM3_TOGP	GTIM2_CH4	GTIM1_CH4	ATIM_CH3	SPI3_MISO	HALLTIM_CH3
PB08	UART2_RXD	UART3_TXD	I2C1_SCL	ADC2_SAM	ATIM_CH4N	GTIM1_CH3	ATIM_ETR	SPI3_SCK	
PB09	UART2_TXD	UART3_RXD	I2C1_SDA	IR_OUT	ATIM_CH4	GTIM1_CH4	ATIM_BK	SPI3_CS	
PB10	UART3_RXD	UART2_RTS	I2C1_SCL	ATIM_BK2	VC4_OUT	GTIM2_CH3	ATIM_CH2	I2C2_SCL	HALLTIM_CH2
PB11	UART1_RXD	ATIM_BK2OUT	I2C1_SDA	LSI_OUT	BTIM1_ETR	GTIM2_CH4	ATIM_CH3	I2C2_SDA	HALLTIM_CH3
PB12	UART1_TXD	LPTIM_OUT	SPI1_CS	LSE_OUT	VC1_OUT	ATIM_TRGO	ATIM_BK	SPI2_CS	HALLTIM_OUT
PB13	UART2_RXD	LPTIM_ETR	SPI1_SCK	ATIM_BK2	VC2_OUT	ATIM_TRGO2	ATIM_CH1N	SPI2_SCK	HALLTIM_CH1
PB14	UART2_TXD	LPTIM_CH2	SPI1_MISO	RTC_OUT	VC3_OUT	GTIM2_CH1	ATIM_CH2N	SPI2_MISO	HALLTIM_CH2
PB15	UART3_RXD	LPTIM_CH1	SPI1_MOSI	RTC_OUT	BTIM2_TOGN	GTIM2_CH2	ATIM_CH3N	SPI2_MOSI	HALLTIM_CH3

Table 5-5 Alternate functions selected through GPIOC_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PC13	MCO_OUT		RTC_TAMP	RTC_OUT	BTIM2_ETR	ATIM_BK	ATIM_ETR	GTIM3_ETR	GTIM4_ETR
PC14	UART1_RXD	UART2_RXD	UART3_CTS	I2C1_SDA	BTIM2_TOGN	ATIM_CH6	ATIM_CH5N	SPI3_MISO	GTIM4_CH1
PC15	UART1_TXD	UART2_TXD	UART3_RTS	I2C1_SCL	BTIM2_TOGP	ATIM_CH6N	ATIM_CH5	SPI3_MOSI	GTIM4_CH2

Table 5-6 Alternate functions selected through GPIOF_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PF00	UART1_RXD			I2C1_SDA	BTIM1_TOGN	GTIM1_TRGO	ATIM_CH6N	SPI3_SCK	GTIM4_CH3
PF01	UART1_TXD	HEXEN	LSE_OUT	I2C1_SCL	BTIM1_TOGP	GTIM2_TRGO	ATIM_CH6	SPI3_CS	GTIM4_CH4
PF03/BOOT	LSE_OUT	LSI_OUT	ADC1_SAM	LVD_OUT	HCLK_OUT	ATIM_TRGO	IR_OUT	GTIM3_TRGO	GTIM4_TRGO
PF06	UART1_CTS	UART3_RXD	UART2_CTS	I2C1_SCL	BTIM3_TOGN	GTIM2_TRGO	ATIM_CH5	I2C2_SCL	GTIM4_TRGO
PF07	UART1_RTS	UART3_TXD	UART2_RTS	I2C1_SDA	BTIM3_TOGP	GTIM1_TRGO	ATIM_CH5N	I2C2_SDA	SPI2_CS

6 Address mapping

Figure 6-1 CW32L012 internal address mapping

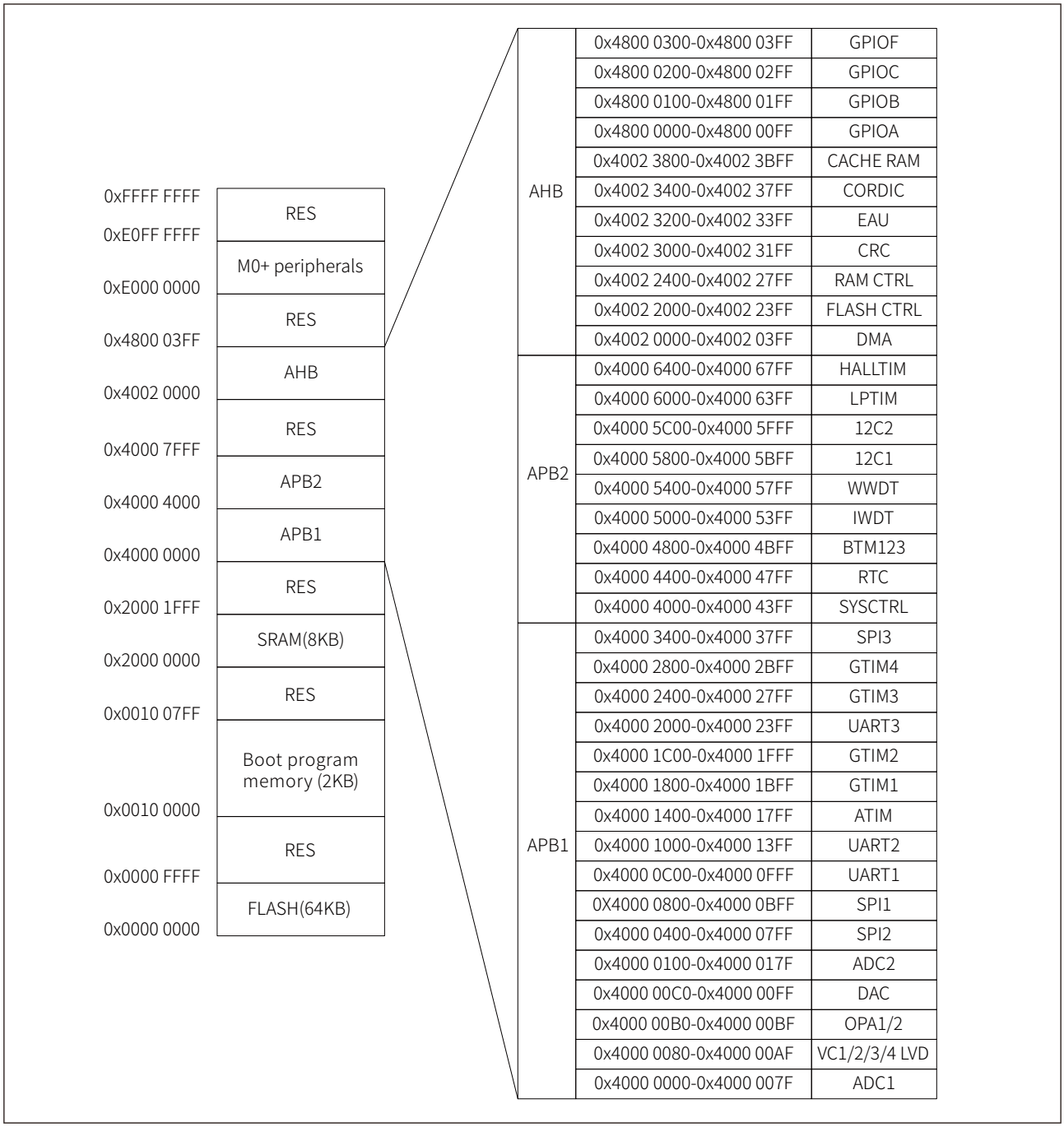


Table 6-1 CW32L012 memory and peripheral register boundary addresses

Device or bus	Boundary address	Size	Peripheral
Main FLASH memory	0x0000 0000 - 0x0000 FFFF	64KB	Main FLASH
Boot program memory	0x0010 0000 - 0x0010 09FF	2KB	BootLoader
OTP memory	0x0010 0760 - 0x0010 0775	22B	OTP
SRAM memory	0x2000 0000 - 0x2000 1FFF	8KB	SRAM
APB1 peripheral	0x4000 0000 - 0x4000 03FF	1KB	ADC12/VC1234/LVD/OPA12/DAC
	0x4000 0400 - 0x4000 07FF	1KB	SPI2
	0x4000 0800 - 0x4000 0BFF	1KB	SPI1
	0x4000 0C00 - 0x4000 0FFF	1KB	UART1
	0x4000 1000 - 0x4000 13FF	1KB	UART2
	0x4000 1400 - 0x4000 17FF	1KB	ATIM
	0x4000 1800 - 0x4000 1BFF	1KB	GTIM1
	0x4000 1C00 - 0x4000 1FFF	1KB	GTIM2
	0x4000 2000 - 0x4000 23FF	1KB	UART3
	0x4000 2400 - 0x4000 27FF	1KB	GTIM3
	0x4000 2800 - 0x4000 2BFF	1KB	GTIM4
	0x4000 3400 - 0x4000 37FF	1KB	SPI3
APB2 peripheral	0x4000 4000 - 0x4000 43FF	1KB	SYSCTRL
	0x4000 4400 - 0x4000 47FF	1KB	RTC
	0x4000 4800 - 0x4000 4BFF	1KB	BTIM123
	0x4000 5000 - 0x4000 53FF	1KB	IWDT
	0x4000 5400 - 0x4000 57FF	1KB	WWDT
	0x4000 5800 - 0x4000 5BFF	1KB	I2C1
	0x4000 5C00 - 0x4000 5FFF	1KB	I2C2
	0x4000 6000 - 0x4000 63FF	1KB	LPTIM
	0x4000 6400 - 0x4000 67FF	1KB	HALLTIM
AHB peripheral	0x4002 0000 - 0x4002 03FF	1KB	DMA
	0x4002 2000 - 0x4002 23FF	1KB	FLASH CTRL
	0x4002 2400 - 0x4002 27FF	1KB	RAM CTRL

Table 6-1 CW32L012 memory and peripheral register boundary addresses (continued)

Device or bus	Boundary address	Size	Peripheral
AHB peripheral (continued)	0x4002 3000 - 0x4002 31FF	0.5KB	CRC
	0x4002 3200 - 0x4002 33FF	0.5KB	EAU
	0x4002 3400 - 0x4002 37FF	1KB	CORDIC
	0x4002 3800 - 0x4002 3BFF	1KB	CACHE_RAM
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA/B/C/F
M0+ peripheral	0xE000 0000 - 0xE00F FFFF	1MB	M0+ peripheral

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3Σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=3.3V. They are given only as design guidelines and are not tested.

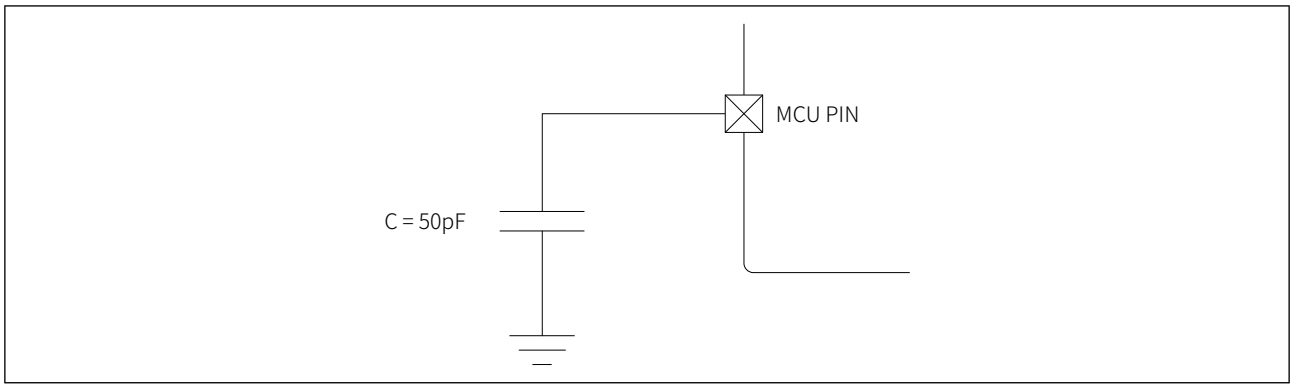
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below:

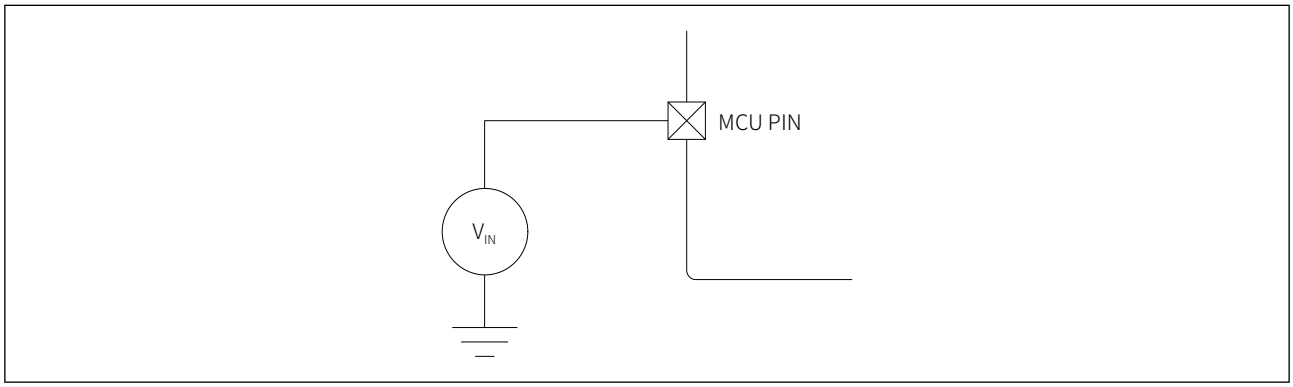
Figure 7-1 Pin loading conditions



7.1.5 Pin input voltage

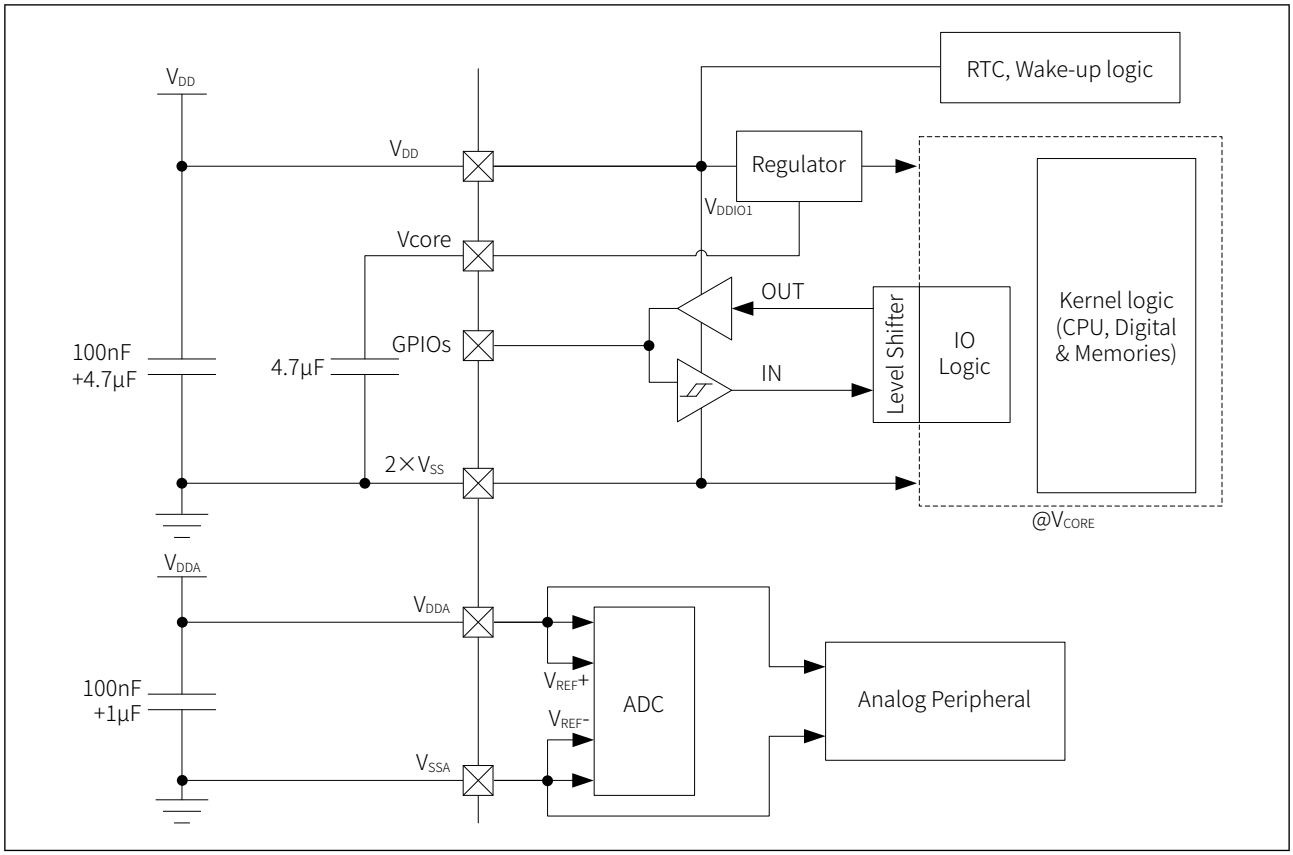
The input voltage measurement on a pin of the device is described in the figure below:

Figure 7-2 Pin input voltage



7.1.6 Power system

Figure 7-3 Power system



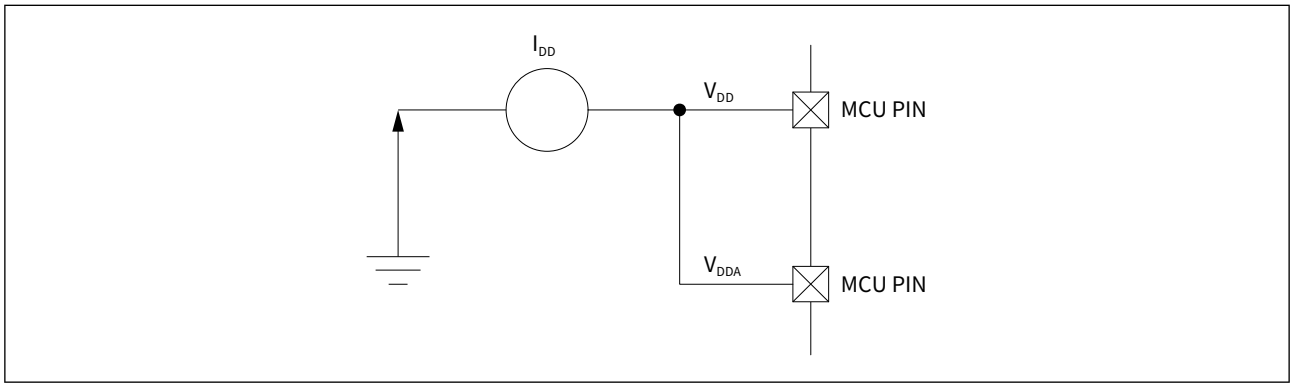
Attention: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Attention: All VDD pins must be powered and at the same voltage.

Attention: Vcore is the regulator supply output and must be connected to a 4.7µF capacitor to ground and is for internal circuit use only.

7.1.7 Current consumption measurement

Figure 7-4 Method of measurement



7.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 7-1, Table 7-2 and Table 7-3 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7-1 Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DD} - V_{SS}	External main supply voltage	-0.3	6.0	V
V_{DDA}-V_{SS}	External analog supply voltage	-0.3	6.0	V
V_{DD}-V_{DDA}	Allowed voltage difference for V_{DD}>V_{DDA}	-	0.3	V
V_{IN} [1]	Input voltage on port IO	V_{SS} - 0.3	V_{DD} + 0.3	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	See Table 7-23: ESD & LU characteristics		kV

[1] V_{IN} maximum must always be respected，refer to Table 7-2: Current characteristics for the maximum allowable injection current value.

Note: All main power (VDD and VDDA) and ground (VSS and VSSA) pins must always be connected to the external power supply, in the permitted range.

Table 7-2 Current characteristics

Symbol	Ratings	Max.	Unit
$I_{VDD(PIN)}$	Total current into sum of a single V_{DD} power lines (source) [1]	+100	mA
$I_{VSS(PIN)}$	Total current out of sum of a single V_{SS} power lines (sink) [1]	-100	
$I_{IO(PIN)}$	Current into a single I/O or control pin	+25	
	Current out of a single I/O or control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os or control pins	+80	
	Total output current sourced by sum of all I/Os or control pins	-80	
$I_{INJ(PIN)}$ [2] [3]	Injected current on TC and RST pins	±5	
	Injected current on TTa pins	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) [4]	±25	

[1] All main power (VDD and VDDA) and ground (VSS and VSSA) pins must always be connected to the external power supply, in the permitted range.

[2] $I_{INJ(PIN)}$ must not exceed its limit to ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed to not to exceed its maximum value, also ensure that external limit $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. When V_{IN}>V_{DD}, there is a forward injection current; when V_{IN}<V_{SS}, there is a reverse injection current.

[3] Negative injection disturbs the analog performance of the device.

[4] When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents. This result is based on the characterization of the maximum value of $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	℃
T_J	Maximum junction temperature	105	

7.3 Operating conditions

7.3.1 General operating conditions

Table 7-4 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{HCLK}	Internal AHB bus frequency	V_{DD}≥1.8V	0	96	MHz
f_{PCLK}	Internal APB bus frequency	V_{DD}≥1.8V	0	96	
f_{HCLK}	Internal AHB bus frequency	1.7V≤V_{DD}<1.8V	0	24	
f_{PCLK}	Internal APB bus frequency	1.7V≤V_{DD}<1.8V	0	24	
V_{DD}	Standard operating voltage	-	1.7	5.5	V
V_{DDA}	Analog operating voltage	Must have a potential equal to V_{DD}	1.7	5.5	V
V_{IN}	I/O input voltage	TC I/O	-0.3	V_{DD} + 0.3	V
		TTa I/O	-0.3	V_{DDA} + 0.3	
P_D	Power dissipation at T_A=+85°C for suffix 6 [1]	LQFP48	-	364	mW
		QFN48	-	714	
T_A	Ambient temperature (suffix 6 version)	Maximum power dissipation	-40	85	°C
		Low power dissipation [2]	-40	105	
T_J	Junction temperature range	Suffix 6 version	-40	105	°C

[1] If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see 8.3 Thermal characteristics).
[2] In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see 8.3 Thermal characteristics).

7.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are tested under the working conditions listed in Table 7-4: General operating conditions.

Table 7-5 Operating conditions at power-up/power-down

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0	10000	μs/V
	V_{DD} fall time rate		20	10000	
t_{VDDA}	V_{DDA} rise time rate	-	0	10000	μs/V
	V_{DDA} fall time rate		20	10000	

7.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are tested under the working conditions listed in Table 7-4: General operating conditions.

Table 7-6 Embedded reset and power control block characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{POR/BOR}$	Power on/brown-out reset threshold	Falling edge	1.45 [1]	1.50	1.55 [2]	V
		Rising edge	1.50 [2]	1.55	1.60	V
$V_{BORhyst}$ [3]	BOR hysteresis	-	-	50	-	mV
$t_{RSTTEMPO}$ [3]	Reset temporization	-	4	6.5	18	ms

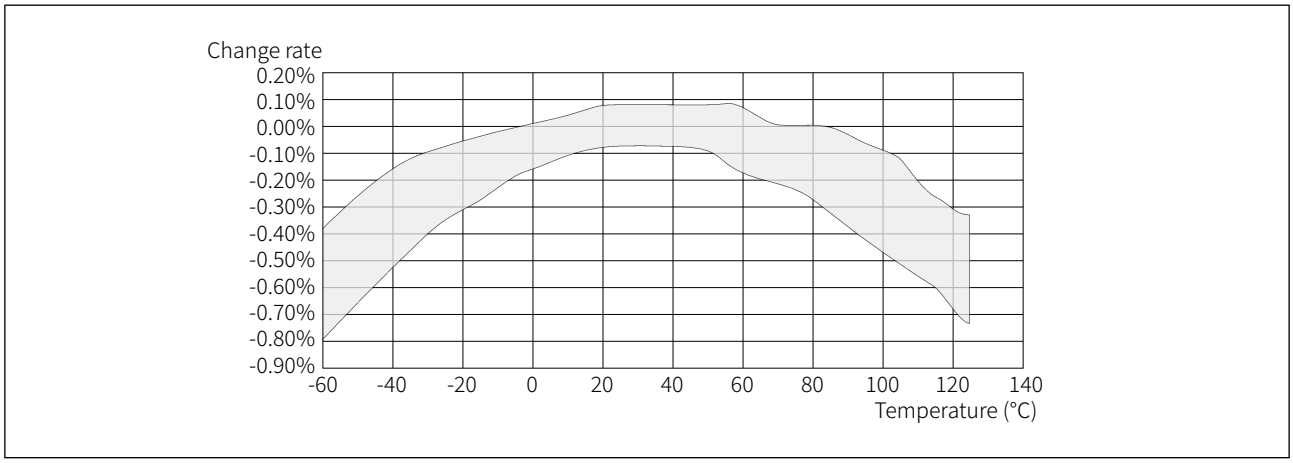
[1] The product behavior is guaranteed by design down to the minimum $V_{POR/BOR}$ value.
[2] Data based on characterization results, not tested in production
[3] Guaranteed by design, not tested in production.

7.3.4 Internal reference voltage

Table 7-7 Internal reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{REFINT1V2}$	Internal 1.2V reference voltage	T_A=-40°C~+85°C		1.2		V
T_{Coeff}	Temperature coefficient	-	-70	-	+70	ppm/°C

Figure 7-5 BGR 1.2V output voltage temperature characteristics



7.3.5 Supply current characteristics

Current consumption is affected by many factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

Figure 7-4: Method of measurement shows the circuit for testing current consumption.

All result of the Run-mode current consumption measurements based on the same limited code used to test CoreMark.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the frequency f_{HCLK}:
  - 0 wait state inserted when 0 to 24MHz
  - 1 wait state inserted when above 24MHz
  - 2 wait state inserted when above 48MHz
  - 3 wait state inserted when above 72MHz
  - 4 wait state inserted when above 96MHz
- When the peripherals are enabled, $f_{PCLK}=f_{HCLK}$

The data given in the following tables are derived from tests performed under the ambient temperature and supply voltage noted in the remarks. For the test conditions, see Table 7-4: General operating conditions:

Table 7-8 Typical and maximum current consumption

Symbol	Parameter	Condition	f_{HCLK}	All peripherals enabled		All peripherals disabled		Unit
				Typ.	Max. [1] T_A=85°C	Typ.	Max. [1] T_A=85°C	
I_{DD} [2]	Supply current in Active mode, (code executing from Flash)	HSI or HSE clock	96MHz	14.5	14.7	5.7	6	mA
			48MHz	8.6	9	4.3	4.5	
			24MHz	5.2	5.5	3.15	3.35	
			12MHz	3	3.15	1.9	2.1	
			8MHz	2.35	2.55	1.65	1.9	
			4MHz	1.7	1.95	1.35	1.6	
I_{DD} [2]	Supply current in Active mode (code executing from RAM)	HSI or HSE clock	96MHz	17.2	18	8.7	9.2	mA
			48MHz	9	9.4	4.6	4.8	
			24MHz	4.65	4.8	2.58	2.7	
			12MHz	2.62	2.8	1.55	1.7	
			8MHz	1.93	2.1	1.21	1.3	
			4MHz	1.23	1.4	0.87	1	
I_{DD} [2]	Supply current in Sleep mode (code executing from Flash or RAM)	HSI or HSE clock	96MHz	11.4	12	2.8	3	mA
			48MHz	6.1	6.3	1.67	1.8	
			24MHz	3.25	3.4	1.1	1.2	
			12MHz	1.88	2	0.93	1.1	
			8MHz	1.45	1.6	0.73	0.9	
			4MHz	1	1.1	0.64	0.75	

[1] Data based on characterization results, not tested in production unless otherwise stated.
[2] I_{DD} is the total current consumption of V_{DD} and V_{DDA}.

Table 7-9 Current consumption when system clock is LSE

Symbol	Parameter	Condition		V_{DD}=1.7V~5.5V		V_{DD}=3.3V	Unit
				Min.	Max. [1]	Typ.	
I_{DD} [2]	Supply current in Active mode (code executing from FLASH, all peripheral clocks enabled)	LSE=32768Hz (DRIVER=0)	T_A=-40°C	-	120	85	μA
			T_A=25°C	-	130	88	
			T_A=50°C	-	135	89	
			T_A=85°C	-	150	100	
	Supply current in Active mode (code executing from FLASH, all peripheral clocks disabled)	LSE=32768Hz (DRIVER=0)	T_A=-40°C	-	110	80	
			T_A=25°C	-	120	82	
			T_A=50°C	-	125	84	
			T_A=85°C	-	145	96	

[1] Data based on characterization results, not tested in production unless otherwise specified.
[2] I_{DD} is the total current consumption of V_{DD} and V_{DDA}.

Table 7-10 Typical and maximum current consumption in DeepSleep

Symbol	Parameter	Condition	Typ. @V_{DD} (V_{DD}=V_{DDA})	Max. [1]	Unit
			3.3V	T_A=85°C	
I_{DD} [2]	Supply current in DeepSleep mode	The regulator is in Active mode, all oscillators are off	0.5	6	μA
		The regulator is in Active mode, LSE, RTC and IWDT are on	1.5	6	

[1] Data based on characterization results, not tested in production unless otherwise stated.
[2] I_{DD} is the total current consumption of V_{DD} and V_{DDA}.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD}=V_{DDA}=3.3V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to thefrequency f_{HCLK}:
  - 0 wait state inserted when 0 to 24MHz
  - 1 wait state inserted when above 24MHz
  - 2 wait state inserted when above 48MHz
  - 3 wait state inserted when above 72MHz
  - 4wait state inserted when above 96MHz
- When the peripherals are enabled, f_{PCLK}=f_{HCLK}

Table 7-11 Typical current consumption in Active mode, program running from FLASH

Symbol	Parameter	Condition	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD} [1]	Supply current in Active mode	Runs from FLASH with 96MHz internal HSIOSC clock	96MHz	14.5	5.7	mA
			48MHz	8.6	4.3	
			24MHz	5.2	3.15	
			12MHz	3	1.9	
			8MHz	2.35	1.65	
			4MHz	1.7	1.35	

[1] I_{DD} is the total current consumption of V_{DD} and V_{DDA}.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

- I/O static current consumption
  All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up resistors values given in Table 7-24: I/O static characteristics.
  For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.
  If the input voltage level of the I/Os is the intermediate voltage level, it will continuously cause the internal Schmitt trigger to flip, resulting in additional random current consumption (although it is small). If it is required to judge the level flip situation in real time, that should configure the I/Os in analog input mode to avoid this.
  Attention: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.
- I/O dynamic current consumption
  In addition to the internal peripheral current consumption measured previously, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW}=V_{DDIOx}\times f_{SW}\times C$$

  where:
  - I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load.
  - V_{DDIOx} is the I/O supply voltage.
  - f_{SW} is the I/O switching frequency.
  - C is the total capacitance seen by the I/O pin: $C=C_{INT}+C_{EXT}+C_S$.
  - C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 7-12 Switching output I/O current consumption

Symbol	Parameter	Condition [1]	I/O toggling frequency (f_{SW})	Typ.	Unit
I_{SW}	I/O current consumption	V_{DDIOx}=3.3V C_{EXT}=0pF $C=C_{INT}+C_{EXT}+C_S$	4MHz	0.18	mA
			8MHz	0.37	
			16MHz	0.76	
			24MHz	1.39	
		V_{DDIOx}=3.3V C_{EXT}=22pF $C=C_{INT}+C_{EXT}+C_S$	4MHz	0.49	
			8MHz	0.94	
			16MHz	2.38	
			24MHz	3.99	
		V_{DDIOx}=3.3V C_{EXT}=47pF $C=C_{INT}+C_{EXT}+C_S$	4MHz	0.81	
			8MHz	1.7	
			16MHz	3.67	

[1] C_S=7pF (estimated value).

7.3.6 Wakeup time from Low-power mode

The wakeup times given in the table below are tested during the wake-up phase of the HSIOSC.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode and DeepSleep mode.

All test environments are from ambient temperature and supply voltage conditions summarized in Table 7-4 : General operating conditions.

Table 7-13 Low-power mode wakeup timings

Symbol	Parameter	Condition	Typ. @V_{DD} (V_{DD}=V_{DDA})	Max.	Unit
			3.3V		
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4	-	HCLK
t_{WUDEEP}	Wakeup form DeepSleep mode	Regulator in Active mode	5.5	6.5	µs

7.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

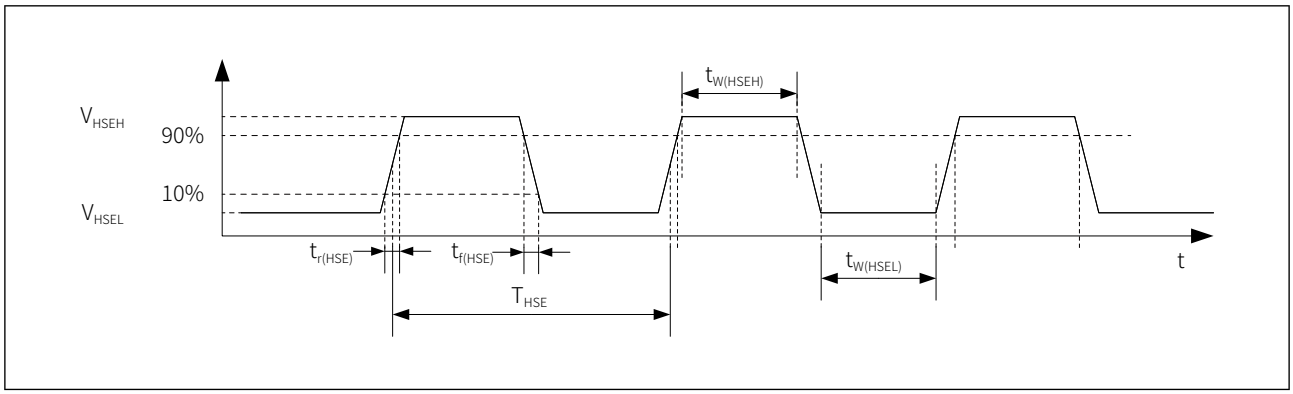
The external clock signal has to respect the I/O characteristics in section 7.3.11 I/O port characteristics. The recommended clock input waveform is shown in the following figure:

Table 7-14 High-speed external clock input characteristics

Symbol	Parameter[1]	Min.	Typ.	Max.	Unit
f_{HSE_EXT}	User external clock source frequency	1	-	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	$0.7V_{DDIOx}$	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	$0.3V_{DDIOx}$	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

[1] Guaranteed by design, not tested in production.

Figure 7-6 High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

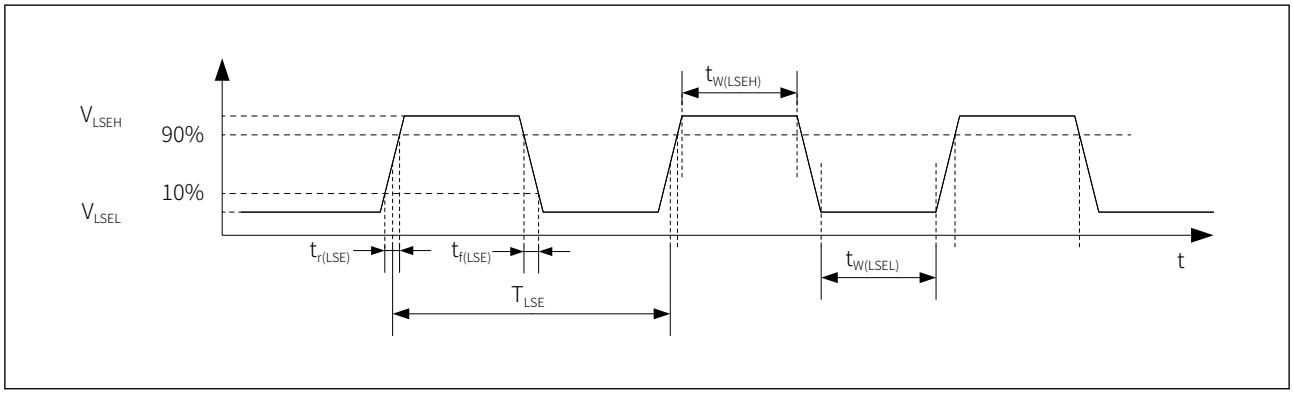
The external clock signal has to respect the I/O characteristics in section 7.3.11 I/O port characteristics. The recommended clock input waveform is shown in the following figure:

Table 7-15 Low-speed external clock input characteristics

Symbol	Parameter [1]	Min.	Typ.	Max.	Unit
f_{LSE_EXT}	User external clock source frequency	-	32.768	100	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	$0.7V_{DDIOx}$	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	$0.3V_{DDIOx}$	
$t_{W(LSEH)}$ $t_{W(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

[1] Guaranteed by design, not tested in production.

Figure 7-7 Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4MHz~32MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 7-16 HSE oscillator characteristics

Symbol	Parameter	Condition [1]	Min. [2]	Typ.	Max. [2]	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
R_F	Feedback resistor	-	-	330	-	kΩ
I_{DD}	HSE current consumption	During startup [3]	-	-	700	μA
		V_{DD}=3.3V, R_m=45Ω, C_L=10pF @8MHz	-	360	-	
		V_{DD}=3.3V, R_m=30Ω, C_L=20pF @32MHz	-	500	-	
$t_{su(HSE)}$ [4]	Startup time	V_{DD} is stabilized	-	2	-	ms

[1] Resonator characteristics given by the crystal/ceramic resonator manufacturer.
[2] Guaranteed by design, not tested in production.
[3] This consumption level occurs during the first 2/3 of the $t_{su(HSE)}$ startup time.
[4] $t_{su(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 7-17 LSE oscillator characteristics (f_{LSE}=32.768kHz)

Symbol	Condition [1]	Condition	Min. [1]	Typ.	Max. [1]	Unit
I_{DD}	LSE current consumption	DRIVER=0	-	0.3	-	μA
		DRIVER=1	-	0.33	-	
		DRIVER=2	-	0.37	-	
		DRIVER=3	-	0.41	-	
		DRIVER=4	-	0.45	-	
		DRIVER=5	-	0.49	-	
		DRIVER=6	-	0.53	-	
		DRIVER=7	-	0.56	-	
		DRIVER=8	-	1.34	-	
		DRIVER=9	-	1.38	-	
		DRIVER=10	-	1.42	-	
		DRIVER=11	-	1.46	-	
		DRIVER=12	-	1.50	-	
		DRIVER=13	-	1.54	-	
		DRIVER=14	-	1.57	-	
		DRIVER=15	-	1.61	-	
$t_{su(LSE)}$ [2]	Startup time	V_{DD} is stabilized	-	1.50	-	s

[1] Guaranteed by design, not tested in production.

[2] $t_{su(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

7.3.8 Internal clock source characteristics

The data given in the following table is based on the sample tests of the test environment indicated by Table 7-4: General operating conditions.

High-speed internal (HSIOSC) RC oscillator

Table 7-18 HSI oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	96	-	MHz
TRIM	HSI user trimming step	-	-	0.2	-	%
$Duty_{HSI}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A=-40°C~+85°C	-2.0	-	+2.0	%
		T_A=-20°C~+50°C	-1.0	-	+1.0	%
		T_A=+25°C	-0.5	-	+0.5	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	6.5	-	8	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	460	-	μA

Low-speed internal (LSI) RC oscillator

Table 7-19 LSI oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	-	32.8	-	kHz
TRIM	LSI user trimming step	-	-	0.16	-	%
$Duty_{LSI}$	Duty cycle	-	30	-	70	%
ACC_{LSI}	Accuracy of the LSI oscillator (factory calibrated)	T_A=-40°C~+85°C	-10	-	+10	%
		T_A=+25°C	-1	-	+1	%
$t_{SU(LSI)}$	LSI oscillator startup time	-	-	-	50	μs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	1	-	μA

Ultra-Low-Speed internal (RC10K) RC Oscillator

Table 7-20 RC10K oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{RC10K}	Frequency	-	-	10.5	-	kHz
$Duty_{RC10K}$	Duty cycle	-	30	-	70	%
ACC_{RC10K}	Accuracy of the RC10K oscillator (factory calibrated)	T_A=-40°C~+85°C	-25	-	25	%
		T_A=+25°C	-5	-	5	%

7.3.9 Memory characteristics

FLASH memory

The characteristics are for -40°C~+85°C test enviroment unless otherwise specified.

Table 7-21 FLASH memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max. [1]	Unit
t_{prog8}	8-bit programming time	T_A=-40°C~+85°C	-	31	-	μs
t_{prog16}	16-bit programming time	T_A=-40°C~+85°C	-	39	-	μs
t_{prog32}	32-bit programming time	T_A=-40°C~+85°C	-	55	-	μs
t_{ERASE}	Page erase time	T_A=-40°C~+85°C	-	2.5	-	ms
t_{ME}	Mass erase time	T_A=-40°C~+85°C	-	35	-	ms
I_{DD}	Supply current	Write mode	-	-	2	mA
		Erase mode	-	-	1	mA

[1] Guaranteed by design, not tested in production.

Table 7-22 FLASH memory endurance and data retention

Symbol	Parameter	Condition	Min. [1]	Unit
N_{NED}	Endurance	T_A=-40°C~+85°C	10	k times
t_{RET}	Data retention	T_A=-40°C~+85°C	25	Years

[1] Obtained by comprehensive evaluation, not tested in production.

7.3.10 ESD & LU characteristics

Use specific measurement methods to test the strength of the chip to determine its electrical sensitivity performance.

Table 7-23 ESD & LU characteristics

Symbol	Parameter	Condition	Typ.	Max.	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25°C, conforming to JS-001: 2023	-	±8	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=+25°C, conforming to JESD22-C101F：2013	-	±2	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A=+25°C, conforming to JESD22-A115C：2010	-	±200	V
LU	Static Latch-Up	T_A=+85°C, conforming to JESD 78F.02：2023	-	±500	mA

7.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by Table 7-4: General operating conditions.

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-24 I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3V_{DDIOx}$	V
V_{IH}	High level input voltage	TC and TTa I/O	$0.7V_{DDIOx}$	-	-	V
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	450[1]	-	mV
I_{ikg}	Input leakage current	TC and TTa I/O in digital mode $V_{SS} \leqslant V_{IN} \leqslant V_{DDIOX}$	-	-	±0.1	μA
		TTa I/O in digital mode $V_{DDIOX} \leqslant V_{IN} \leqslant V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \leqslant V_{IN} \leqslant V_{DDA}$	-	-	±0.2	
R_{PU}[2]	Weak pull-up equivalent resistor	$V_{IN}=V_{SS}$	55	-	70	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

[1] Data based on design simulation only. Not tested in production.

[2] Pull-up resistors is designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal.

Output driving current

The GPIOs can sink or source up to ±8mA, and sink or source up to ±20mA with a relaxed V_{OH} and V_{OL}.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in section 7.2 Absolute maximum ratings:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see Table 7-1: Voltage characteristics).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 7-1: Voltage characteristics).

Output voltage levels

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by Table 7-4: General operating conditions.

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-25 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OH}	High-level output voltage source current	Sourcing 10mA, V_{DD}=3.3V [1]	2.95	-	V
		Sourcing 20mA, V_{DD}=3.3V [2]	2.55	-	
V_{OL}	Low-level output voltage sink current	Sinking 10mA, V_{DD}=3.3V [1]	-	0.28	
		Sinking 20mA, V_{DD}=3.3V [2]	-	0.60	

[1] The maximum total current I_{OH}(max) and I_{OL}(max) of all output combinations should not exceed 40mA to meet the maximum specified voltage drop.

[2] The maximum total current I_{OH}(max) and I_{OL}(max) of all output combinations should not exceed 100mA to meet the maximum specified voltage drop.

Input/output AC characteristics

The values and definitions of the AC characteristics of the I/Os are given by the following charts respectively.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by Table 7-4: General operating conditions.

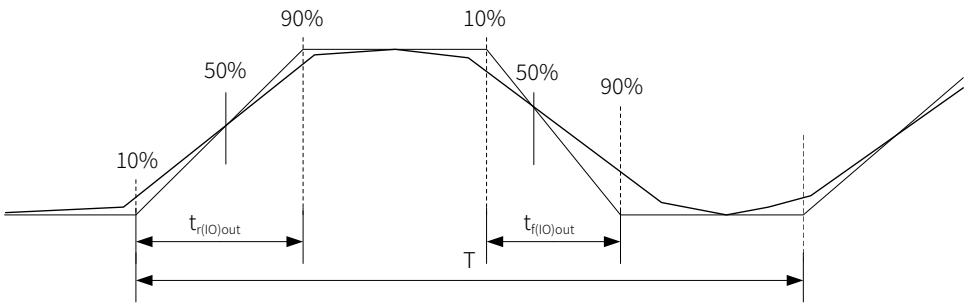
Table 7-26 I/O AC characteristics

Symbol	Parameter	Condition	Min.	Max. [1]	Unit
$f_{max(IO)out}$	Maximum frequency [2]	C_L=30pF, V_{DDIOx}≥2.7V	-	50	MHz
		C_L=50pF, V_{DDIOx}≥2.7V	-	30	
		C_L=50pF, 2.4V≤V_{DDIOx}<2.7V	-	20	
$t_{f(IO)out}$	Output fall time	C_L=30pF, V_{DDIOx}≥2.7V	-	5	ns
		C_L=50pF, V_{DDIOx}≥2.7V	-	8	
		C_L=50pF, 2.4V≤V_{DDIOx}<2.7V	-	12	
$t_{r(IO)out}$	Output rise time	C_L=30pF, V_{DDIOx}≥2.7V	-	5	
		C_L=50pF, V_{DDIOx}≥2.7V	-	8	
		C_L=50pF, 2.4V≤V_{DDIOx}<2.7V	-	12	

[1] Data based on design simulation only, not tested in production.

[2] The maximum frequency is defined in the figure below.

Figure 7-8 I/O AC characteristics definition



Maximum frequency is achieved if (t_r+t_f) ⩽ 2/3T and if the duty cycle is (45-55%) when loaded by C_L.

7.3.12 NRST pin characteristics

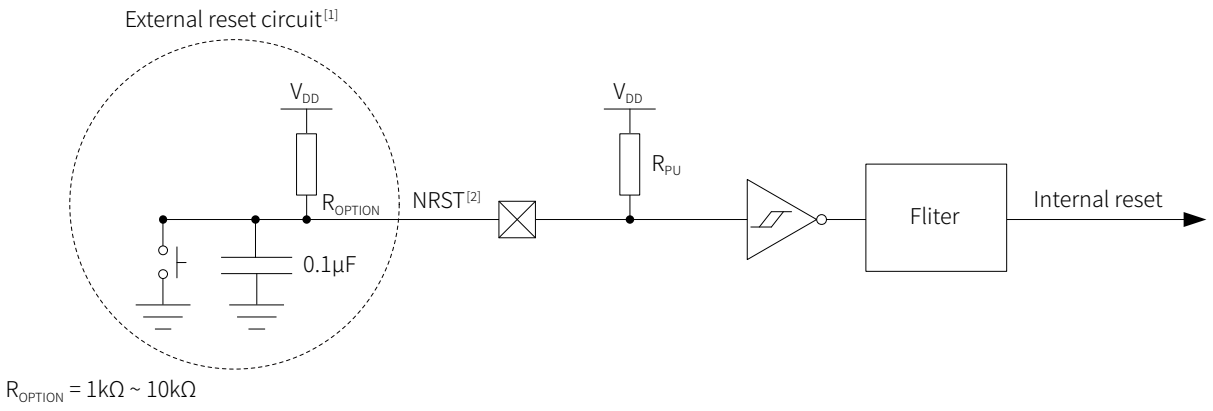
The NRST pin is connected to a permanent pull-up resistor RPU internally.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by Table 7-4: General operating conditions.

Table 7-27 NRST pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3V_{DD}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7V_{DD}$	-	-	
$V_{hys(NRST)}$	NRST input voltage hysteresis	-	-	500	-	mV
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	-	7.3	-	kΩ
$V_{F(NRST)}$	Minimum required reset pulse width	-	20	-	-	μs

Figure 7-9 Recommended NRST pin protection



[1] The external capacitor protects the device against parasitic resets.

[2] The user must ensure that the level on the NRST pin can go below the VIL(NRST) max level specified in $V_{IL(NRST)}$. Otherwise the reset will not be taken into account by the device.

7.3.13 12-bit ADC characteristics

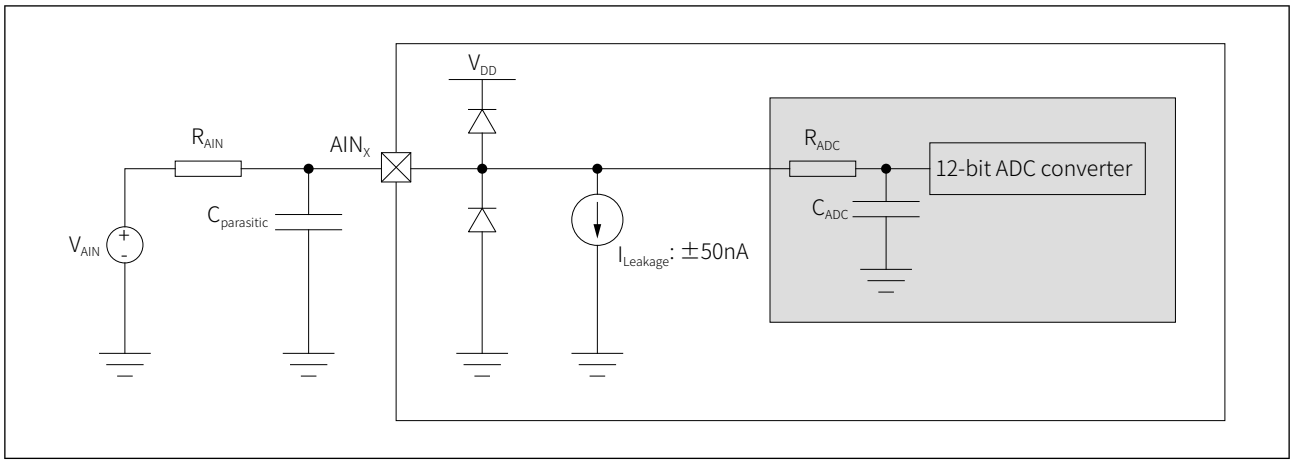
Unless otherwise stated, the test data given in the table below is based on the test environment indicated by Table 7-4: General operating conditions:

Table 7-28 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage for ADC ON	-	1.7	-	5.5	V
$I_{DDA(ADC)}$	Current consumption of ADC	V_{DD}=V_{DDA}=3.3V	-	500	-	μA
f_{ADC}	ADC clock frequency	-	4	48	96	MHz
f_S	Sampling rate	-	-	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 48MHz	-	-	1.6	MHz
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
C_{ADC}	Internal sample and hold capacitor	-	-	4	-	pF
t_S	Sampling time	1.7V<V_{DD}<1.8V	1	-	-	μs
		1.8V<V_{DD}<2.8V	0.5	-	-	μs
		2.8V<V_{DD}<3.3V	0.25	-	-	μs
		3.3V<V_{DD}<5.5V	0.125	-	-	μs
t_{STAB}	Stabilization time	-	15			$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	-	21	-	405	$1/f_{ADC}$

A typical ADC application is shown below:

Figure 7-10 Typical application of ADC



The following formula is used to calculate the maximum value of the external input impedance so that the sampling error can be less than 0.5 LSB:

$$R_{AIN}=M/(f_{ADCCLK}\times C_{ADC}\times(N+1)\times \ln 2)-R_{ADC}$$

Where f_{ADCCLK} is the ADC operating clock frequency, configured by the ADC_CR.CLK bit field; M is the number of sampling clocks, configured by the ADC_SAMPLE.SQRCHy bit field; N is the ADC resolution, and N=12.

Table 7-29 Accuracy of ADC

Symbol	Parameter	Condition	Min.	Typ.	Max.[1]	Unit
ET	Composite error	f_{ADC}=48MHz, V_{DD}=1.7V~5.5V, T_A=-40°C~+85°C	-	±2.5	±3.0	LSB
EO	Offset error		-	±1.5	±2.4	
EG	Gain error		-	±2.2	±2.7	
DNL	Differential nonlinearity		-	±1.0	±2.0	
INL	Integral nonlinearity		-	±3.0	±5.0	
SINAD	Signal-to-noise ratio distortion		-	67	-	dB
SNR	Signal-to-noise ratio		-	70	-	
THD	Total harmonic distortion		-	-70	-	
ENOB	Significant digits	V_{DDA}=1.8V	-	8.6	-	bits
		V_{DDA}=2.8V	-	10.0	-	
		V_{DDA}=3.3V	-	10.2	-	
		V_{DDA}=5.5V	-	10.6	-	

[1] Data based on characterization results, not tested in production.

Attention: ADC DC accuracy values are measured after internal calibration.

Attention: Avoid injecting reverse current on any analogue input pin as this can degrade the accuracy of conversions performed on another analogue input, it is recommended to add a Schottky diode (between the pin and ground) to the analogue pin where the reverse current will probably be injected.

Attention: Better performance can be achieved over restricted V_{DDA}, frequency, and temperature ranges.

7.3.14 12-bit DAC characteristics

Table 7-30 DAC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage for DAC ON	-	1.7	-	5.5	V
V_{REF}	Current consumption of DAC	-	1.7	-	V_{DDA}	V
I_{DDA} [1]	Power consumption	$V_{DD} = V_{DDA} = 3.3V$, CODE=0xFFF, no load	-	30	-	μA
R_O	DAC output impedance	$V_{DD} = V_{DDA} = 3.3V$, CODE = 0xFFF, load resistance 50kΩ	-	4180	-	Ω
R_L [2]	Output resistive load	$V_{DD} = V_{DDA} = 3.3V$, CODE = 0xFFF	5	-	-	kΩ
C_L [2]	Output capacitive load	$V_{DD} = V_{DDA} = 3.3V$, CODE = 0xFFF, load resistance 50kΩ	-	-	50	pF
t_{START} [3]	Set-up time	$V_{DD} = V_{DDA} = 3.3V$, CODE = 0xFFF, $C_{LOAD} \leqslant 50pF$, $R_{LOAD} \geqslant 5k\Omega$	-	3	-	μs
V_{DACOUT}	DAC output voltage (min)	$V_{DD} = V_{DDA} = 1.7V$, CODE = 0x000	-	0.01	-	mV
	DAC output voltage (max)	$V_{DD} = V_{DDA} = 5.5V$, CODE = 0xFFF	-	V_{REF} - 3LSB	-	V
E_O [3]	Offset error	$V_{DD} = V_{DDA} = 3.3V$, CODE = 0x000	-	0.01	-	mV
E_G [3]	Gain error	$V_{DD} = V_{DDA} = 3.3V$, CODE = 0xFFF	-	2.5	-	mV
DNL [3]	Differential nonlinearity	$V_{DD} = V_{DDA} = 3.3V$, no load	-	-	1.5	LSB
INL [3]	Integral nonlinearity	$V_{DD} = V_{DDA} = 3.3V$, no load	-	-	3	LSB

[1] When the DAC maintains a stable value at the output, it is in "static mode", and thus no dynamic consumption is involved.
[2] Data based on design simulation only, not tested in production.
[3] Data based on characterization results, not tested in production.

7.3.15 Temperature sensor characteristics

Table 7-31 TS characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L	V_{SENSE} linearity with temperature	-	±2	±5	°C
Avg_Slope	Average slope	2.52	2.55	2.58	mV/°C
V_{25}	Voltage at 25°C (±5°C)	0.75	0.77	0.79	V
t_{START}	TS internal temperature sensor settling time	-	-	40	μs

7.3.16 Analog voltage comparator characteristics

Table 7-32 Comparator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max. [1]	Unit
V_{DDA}	Supply volgate	-	1.7	-	5.5	V
V_{IN}	Input volgate range	-	0	-	V_{DDA}	V
t_{START}	Startup time	Low speed	-	0.5	-	μs
		High speed	-	0.5	-	
t_D	Delay time	Low speed	-	3	9	
		High speed	-	0.1	0.2	
V_{offset}	Offset errorCurrent consumption	Low speed	-	±4	±15	mV
		High speed	-	±4	±15	
$I_{DD(VC)}$	Comparator hysteresis	Low speed [2]	-	0.25	0.45	μA
		High speed [3]	-	39	55	
V_{hys}	Supply volgate	VCx_CR0.HYS=0	-	0	-	mV
		VCx_CR0.HYS=1	-	26	-	

[1] Data based on characterization results, not production tested.
[2] This power dissipation increases by 21μA~29μA when the negative source is selected with a built-in 1.2V reference.
[3] This power consumption consists of two parts: the VC's own power consumption and the BGR module power consumption.

7.3.17 Programmable low voltage detector characteristics

Table 7-33 Programmable low voltage detector characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	-	0	-	V_{DD}	V
V_{TH}	Detection threshold	LVD_CR0.VTH = 0	0.95 V_{TH}	1.8	1.05 V_{TH}	
		LVD_CR0.VTH = 1		2.2		
		LVD_CR0.VTH = 2		2.6		
		LVD_CR0.VTH = 3		3.0		
		LVD_CR0.VTH = 4		3.4		
		LVD_CR0.VTH = 5		3.8		
		LVD_CR0.VTH = 6		4.2		
		LVD_CR0.VTH = 7		4.6		
I_{DD}	Power consumption	-	-	760	-	nA
t_{resp}	Response time	-	-	32	-	μs
t_{setup}	Set-up time	-	-	100	-	μs
V_{hys}	Hysteresis voltage	-	-	40	-	mV

7.3.18 Operational amplifier characteristic

Table 7-34 Operational amplifier characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	-	0	-	V_{DDA}	V
V_{OUT}	Output voltage	-	0.1	-	V_{DDA} -0.1	V
I_{OUT}	Output current [1]	-	-	-	6	mA
I_{DDA}	Power consumption [2]	-	0.7	-	1.45	mA
R_L	Load resistance	Output deviation < 1%	8	-	-	kΩ
T_{START}	Initialization time	-	2.5	-	-	μs
V_{OS}	Input offset voltage [2]	-	-	1	-	mV
V_{OS}	Input offset voltage [3]	-	-2.5	-	2.5	mV
UGBM	Unit-gain bandwidth [4]	-	-	11	-	MHz
SR	Slew rate	-	-	10	-	V/μs
PGA	Gain	-	1	-	32	-

[1] In the condition of V_{IN} = 3.3V.
[2] In the condition of OPA_CR.BIAS = 111.
[3] In the conditions of 2.4V≤V_{IN}≤5V, and OPA_CR.BIAS = 111.
[4] In the conditions of OPA without external resistors, and OPA_CR.BIAS = 111.

7.3.19 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to section 7.3.11 I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 7-35 Timer characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$T_{res(TIM)}$	Timer resolution	-	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 48MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency	-	-	-	$f_{TIMCLK}/2$	MHz
t_{MAX_COUNT}	Maximum period	-	-	-	65536	t_{TIMCLK}

Table 7-36 IWDT min/max timeout period at 10kHz (RC10K)

Frequency division factor	IWDT_CR.PRS	Min timeout period	Max timeout period	Unit
4	0	0.381	1560	ms
8	1	0.762	3121	
16	2	1.524	6242	
32	3	3.048	12483	
64	4	6.095	24966	
128	5	12.190	49932	
256	6	24.381	99864	
512	7	48.762	199728	

Table 7-37 WWDT min/max timeout period at 48MHz (PCLK)

Frequency division factor	Control bit	Min timeout period	Max timeout period	Unit
4096	0	0.086	3.413	ms
8192	1	0.171	6.826	
16384	2	0.342	13.653	
32768	3	0.683	27.306	
65536	4	1.366	54.613	
131072	5	2.731	109.226	
262144	6	5.461	218.428	
524288	7	10.923	436.906	

7.3.20 Communication interfaces

I2C interface characteristics

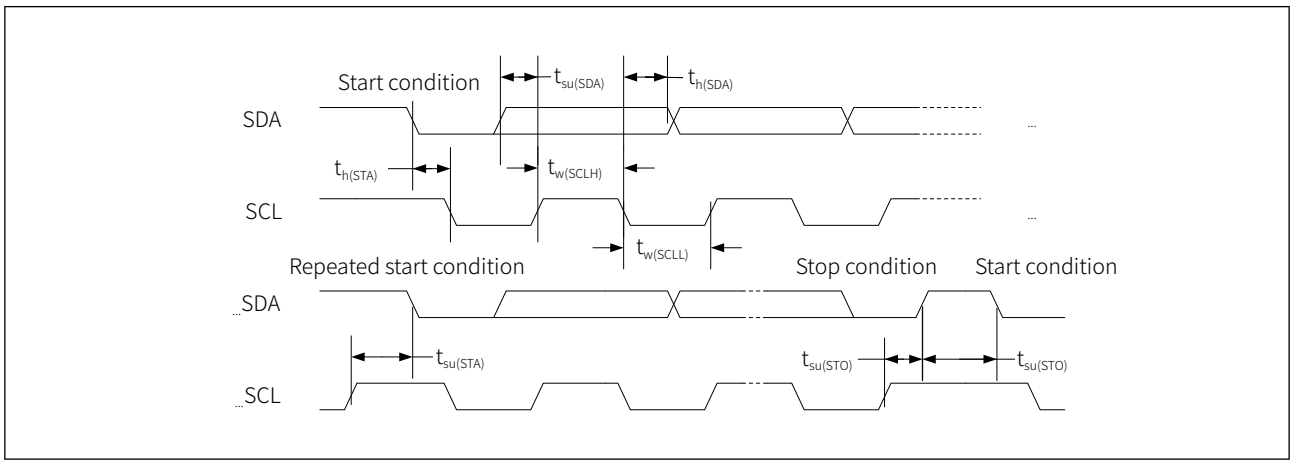
- The I2C interface meets the I2C-bus specification and the user manual:
  - Standard-mode(Sm): with a bit rate up to 100kbit/s
  - Fast-mode(Fm): with a bit rate up to 400kbit/s
  - Fast-mode Plus(Fm+): with a bit rate up to 1Mbit/s
- The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).
- The SDA and SCL I/O requirements are met with the following restrictions:
  - The SDA and SCL I/O pins are not "true" open-drain, maximum input voltage limited by specification. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present.

Refer to section 7.3.11 I/O port characteristics for the I2C I/Os characteristics.

Table 7-38 I2C characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.25	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	50	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{h(STA)}$	Start condition hold time	2.5	-	0.625	-	0.25	-	μs
$t_{su(STA)}$	Repeated start condition startup time	2.5	-	0.6	-	0.25	-	
$t_{su(STO)}$	Stop condition setup time	0.25	-	0.25	-	0.25	-	
$t_{w(STO:STA)}$	Stop condition to start condition time (Bus Idle)	4.7	-	1.3	-	0.5	-	

Figure 7-11 I2C timing diagram



SPI interface characteristic parameters

Table 7-39 SPI characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{c(SCK)}$	SPI clock frequency	Master mode	-	24	ns
		Slave mode	-	18	
$t_{su(NSS)}$	NSS setup time	Slave mode	1×t_{PCLK}	-	
$t_{h(NSS)}$	NSS hold time	Slave mode	1.0	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low setup time	Master mode/ Slave mode	0.5×$t_{c(SCK)}$	-	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	1.0	-	
		Slave mode	1.0	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	1.0	-	
		Slave mode	2.0	-	
$t_{v(SO)}$	Data output valid time	Master mode	-	10.0	
$t_{h(MO)}$	Data output hold time	Slave mode	2.1	-	

Figure 7-12 SPI timing diagram - slave mode and CPHA=0

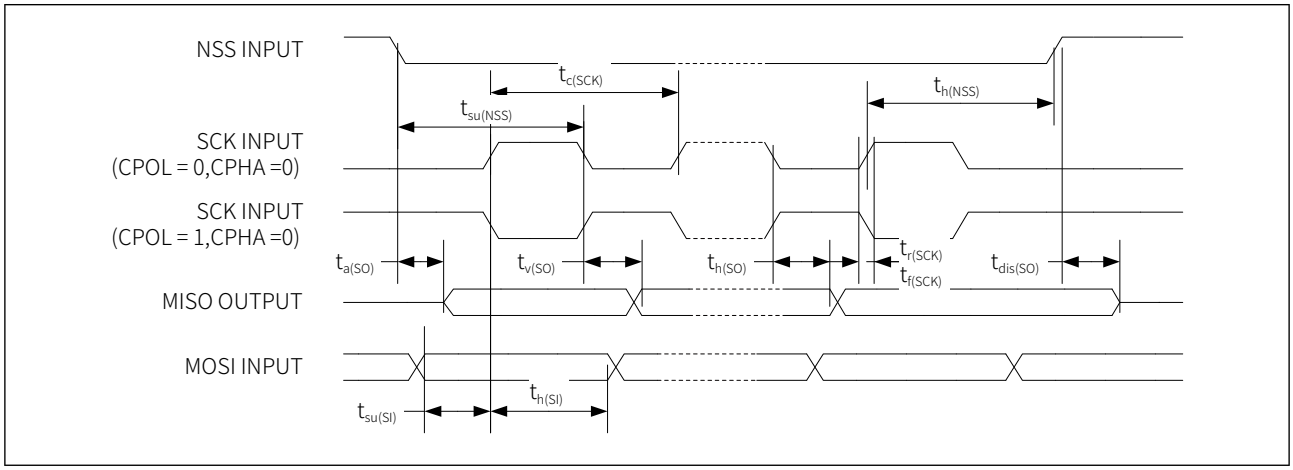


Figure 7-13 SPI timing diagram - slave mode and CPHA=1

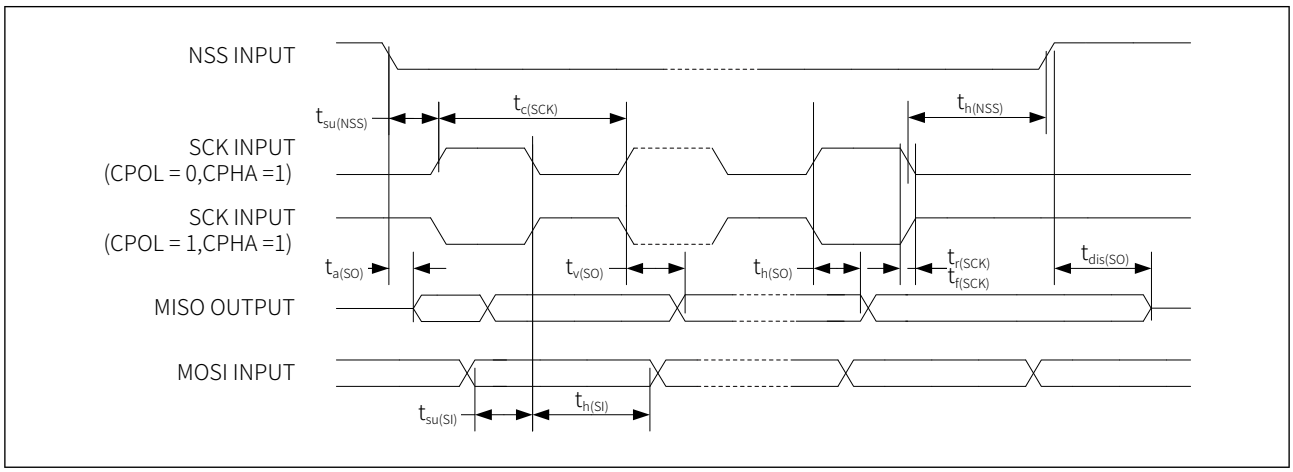
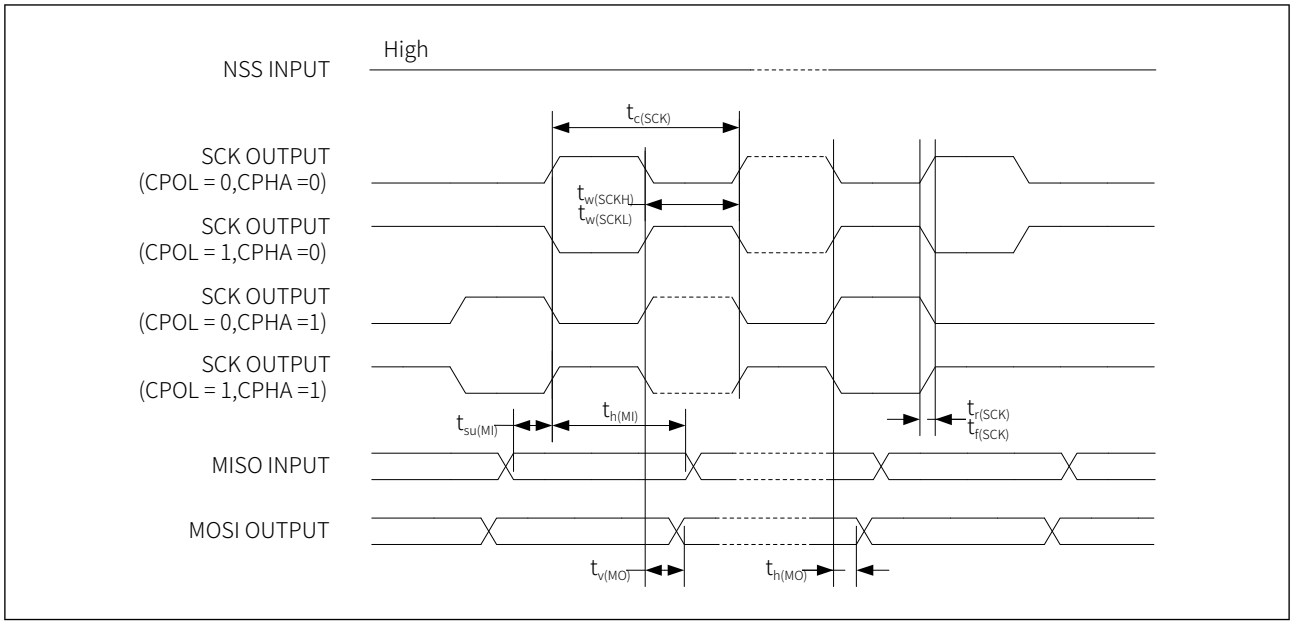


Figure 7-14 SPI timing diagram - master mode

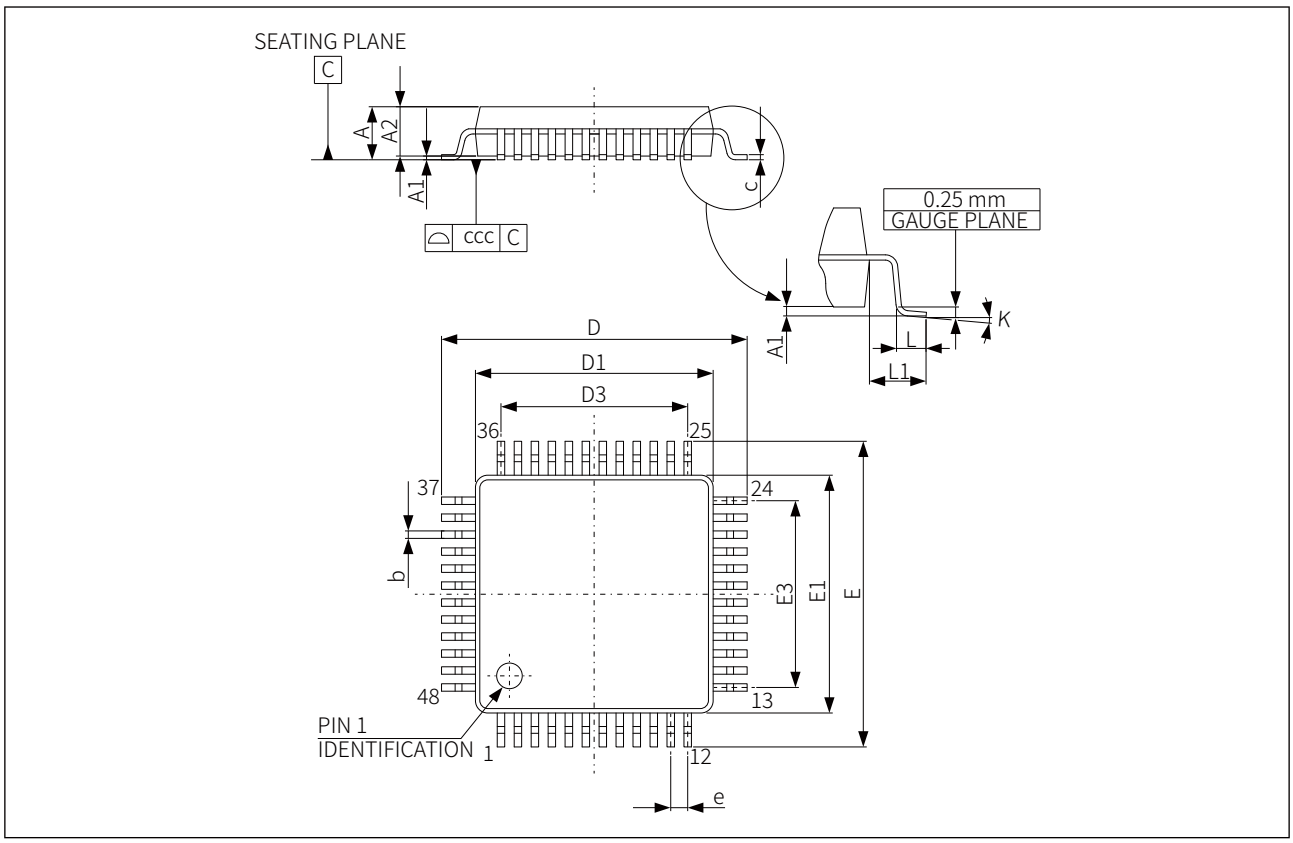


8 Package information

8.1 LQFP48 package information

LQFP48 is 48-pin, 7×7mm low-profile quad flat package.

Figure 8-1 LQFP48 outline



Attention: Drawing is not to scale.

Table 8-1 LQFP48 mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

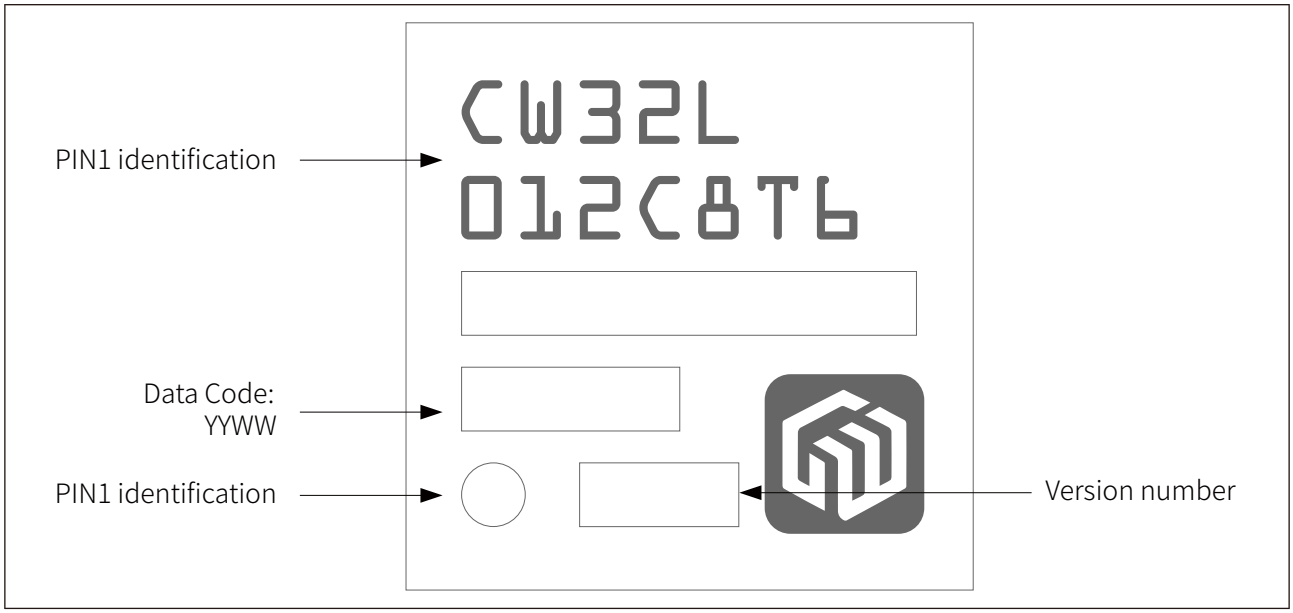
[1] Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-2 LQFP48 topside marking example

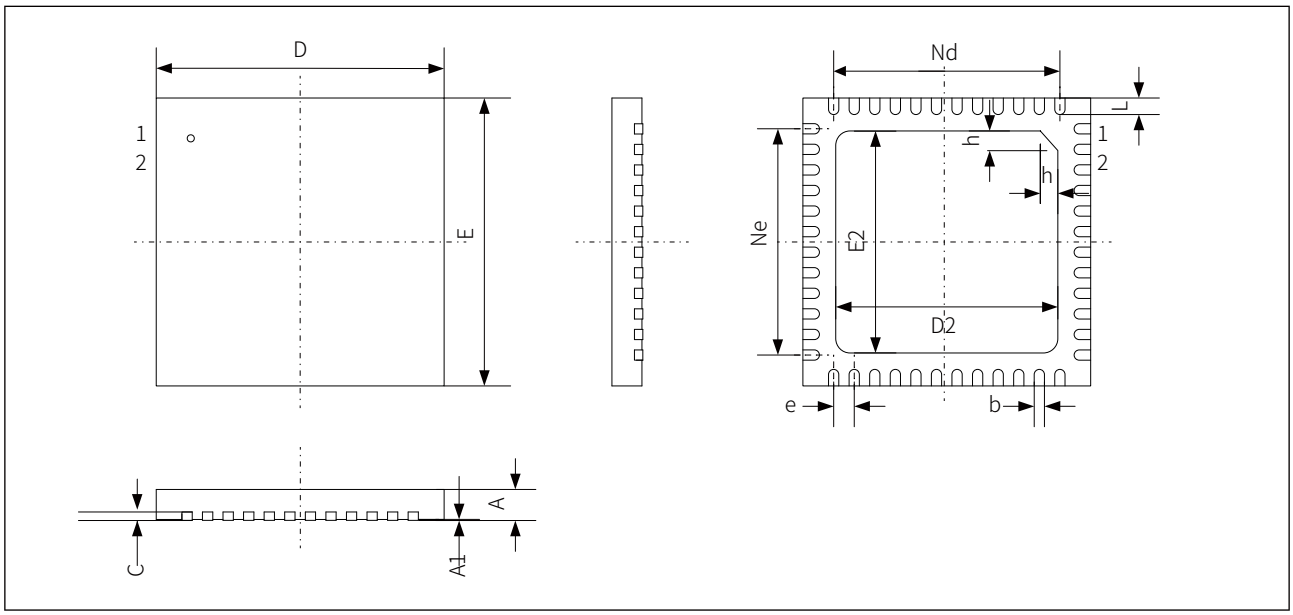


Attention: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.2 QFN48 package information

QFN48 is 48-pin, 7×7mm quad flat no-leads package.

Figure 8-3 QFN48 outline



Attention: Drawing is not to scale.

Table 8-2 QFN48 mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	-	0.02	0.05	-	0.0008	0.0020
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
c	0.18	0.20	0.23	0.0071	0.0079	0.0091
D	6.90	7.00	7.10	0.2717	0.2756	0.2795
D2	5.30	5.40	5.50	0.2087	0.2126	0.2165
e		0.50 BSC			0.0197 BSC	
Ne		5.50 BSC			0.2165 BSC	
Nd		5.50 BSC			0.2165 BSC	
E	6.90	7.00	7.10	0.2717	0.2756	0.2795
E2	5.30	5.40	5.50	0.2087	0.2126	0.2165
L	0.35	0.40	0.45	0.0138	0.0157	0.0177
h	0.30	0.35	0.40	0.0118	0.0138	0.0157

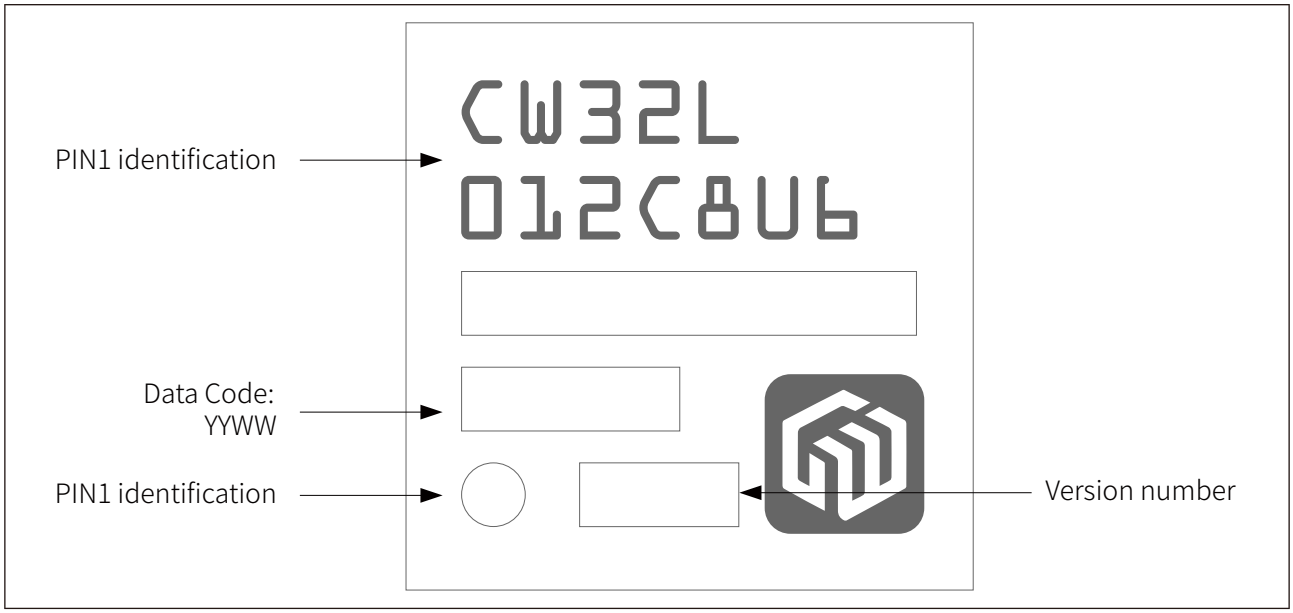
[1] Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-4 QFN48 topside marking example



Attention: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.3 Thermal characteristics

The maximum chip junction temperature $T_J$max must never exceed the values given in Table 7-3: Thermal characteristics.

The maximum chip-junction temperature, $T_J$max, in degrees Celsius, may be calculated using the following equation:

$$T_J\text{max}=T_A\text{max}+（P_D\text{max}\times\Theta_{JA}）$$

Where:

- $T_A$max is the maximum ambient temperature in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.
- $P_D$max is the sum of P_{INT}max and $P_{I/O}$max ($P_D\text{max}=P_{INT}\text{max}+P_{I/O}\text{max}$).
- P_{INT}max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.
- $P_{I/O}$max represents the maximum power dissipation on output pins, where:

$$P_{I/O}\text{max}=\Sigma\ (V_{OL}\times I_{OL}\ )+\Sigma\ ((V_{DD}-V_{OH})\times I_{OH})$$

The actual level and current conditions of the I/Os need to be included in the accurate calculation.

Table 8-3 Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48 – 7mm×7mm	55	°C/W
	Thermal resistance junction-ambient QFN48 – 7mm×7mm	28	

8.3.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org。

9 Ordering information

Example: CW32L012C8T6x

Device family
CW32=ARM-based

Product type
L=Lower power

Sub-family
012=CW32L012xx

Pin count
F=20 pins
K=32 pins
C=48 pins
Y=16 pins

Code size
6=32Kbytes Flash
8=64Kbytes Flash

Package
M=SOP
P=TSSOP
T/S=LQFP
U/V=QFN

Temperature range
6=-40°C~85°C
7=-40°C~105°C

Option
xxx=Programmed part
TR=Tape and reel

Table 9-1 Minimum Order Quantity (MOQ)

MCU	Packaging	Quantity	MOQ	MSL	Note
CW32L012C8T6	Tray	250 pcs/tray	2500 pcs	3	10 trays/box, 6 boxes/carton, single box vacuumized
CW32L012C8U6	Tray	260 pcs/tray	2600 pcs	3	10 trays/box, 6 boxes/carton, single box vacuumized

10 Revision history

Table 10-1 Document revision history

Date	Revision	Changes
January 16, 2026	Rev 1.0	Initial release.