武汉芯源半导体有限公司
WUHAN XINYUAN SEMICONDUCTOR CO., LTD

CW32L010 Datasheet

ARM® Cortex®-M0+ 32-bit low power MCU with up to 64KB FLASH, 4KB RAM

Rev 1.0

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Contents

1 Features

- Core: ARM® Cortex®-M0+
  - Frequency up to 48 MHz
- Operating temperature: -40°C to 85°C ; Operating voltage: 1.62V to 5.5V
- Memories
  - Maximum 64K bytes FLASH, data retention for 25 years @-40°C ~ +85°C , support erase protection, read protection and safe runtime protection
  - Up to 4K bytes RAM, support hardware parity check
  - 22 bytes OTP memory
- CRC calculation unit
- Reset and power management
  - Low power modes (Sleep, DeepSleep)
  - Power-on/ brown-out reset (POR/BOR)
  - Programmable low voltage detector (LVD)
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32kHz low speed crystal oscillator
  - Internal 48MHz RC oscillator
  - Internal 32kHz RC oscillator
  - Clock monitoring system
  - Allow independent shutdown of each peripheral clock
- Up to 16 I/O ports, 1 input port
  - All I/O ports support filtered interrupt function.
  - All I/O ports support filtered wake-up function.
  - All I/O ports support hysteresis and pull-up input.
  - All I/O ports support push-pull and open-drain output.
- 12-bit ADC
  - Up to 2M SPS conversion speed, sample time for each sequence channel can be configured separately
  - 8 conversion result registers
  - Built-in 1.2V voltage reference
  - Analog watchdog function
  - Built-in temperature sensor
- Dual voltage comparator
- Real Time Clock and Calendar
  - Support wakeup from Sleep/DeepSleep mode

- Timers
  - One 16-bit advanced-control timer, support 6-input capture, support 6 pairs of complementary PWM outputs with dead zone, support two-point comparison, support PWM phase shift
  - A group of 16-bit general-purpose timer
  - Three groups of 16-bit basic timers
  - A group of 16-bit low power timer
  - Independent watchdog timer
- Communication interfaces
  - Two low-power UARTs, support fractional baud rate, support low-power receive data, support configurable level shifting, one of them supports LIN communication interface.
  - One SPI interface 24Mbit/s, support 4~16bit bit width
  - One I2C interface 1Mbit/s, supports configurable level shifting, supports SMBUS
  - IR modulator, programmable duty cycle and polarity
- Serial wire debug (SWD)
- 80-bit unique ID

Table 1-1 Package model list

Series	Model	Package
CW32L010x8	CW32L010F8	QFN20
		TSSOP20
	CW32L010Y8	SOP16

2 Introduction

This datasheet provides the ordering information and electromechanical characteristics of the CW32L010 microcontrollers.

This document should be read in conjunction with the CW32L010 reference manual.

For information on the Arm® Cortex®-M0+ core, please refer to the Cortex®-M0+ Technical Reference Manual, available from the *www.arm.com*.

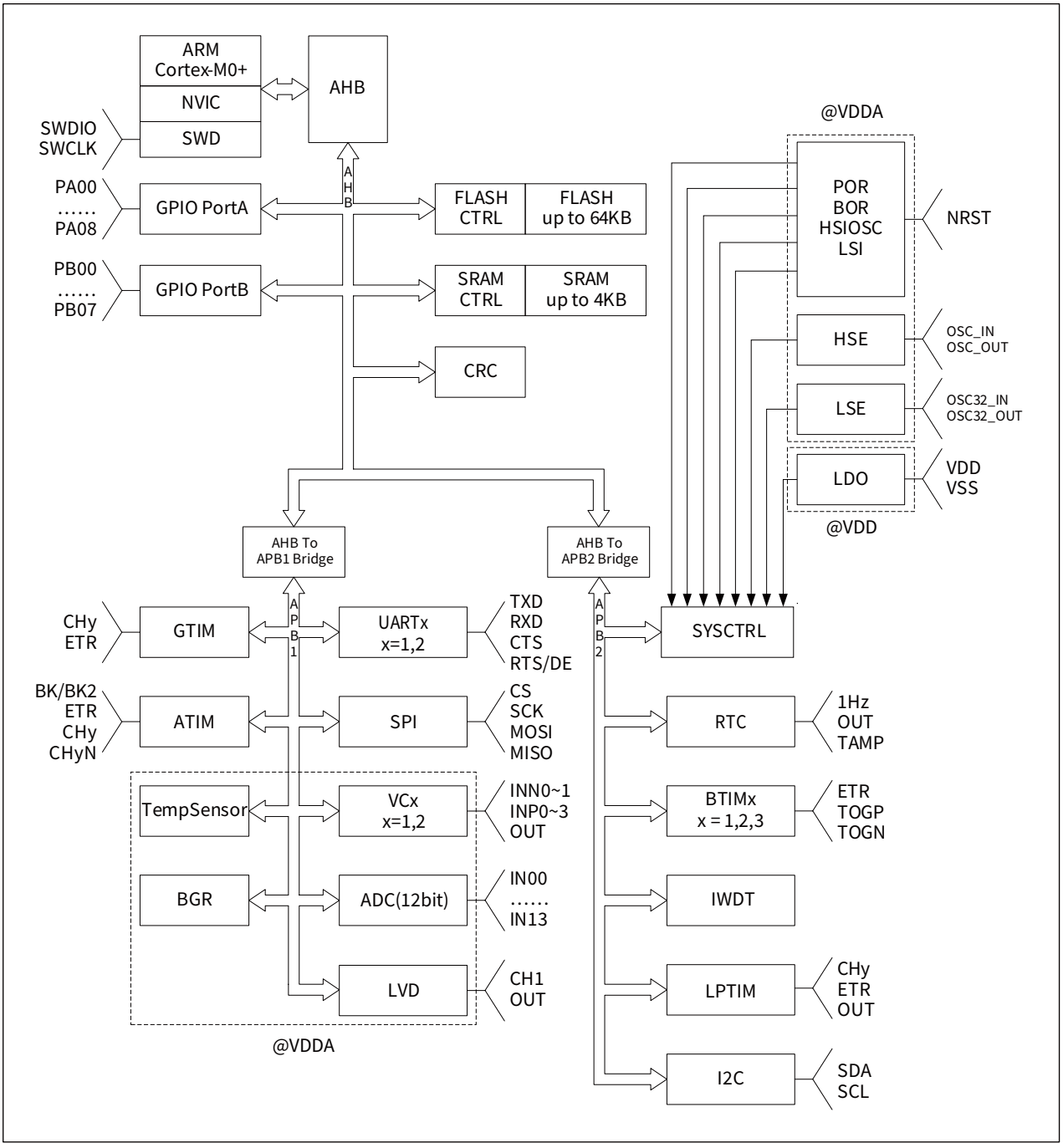
3 Description

CW32L010 is an eFlash-based single-chip Low-Power microcontroller that integrates an ARM® Cortex®-M0+ core with a main frequency up to 48MHz, high-speed embedded memories (up to 64K bytes of FLASH and up to 4K bytes of SRAM), and an extensive range of enhanced peripherals and I/Os.

All devices offer standard communication interfaces (two UARTs, one SPI, one I2C), one 12-bit ADC, four general-purpose and basic timers, one low-power timer and one advanced-control PWM timer.

CW32L010 operates in the -40°C to 85°C temperature range from a 1.62 to 5.5V power supply, supports two low-power operating modes (Sleep and DeepSleep). The internal block diagram is shown in the following figure:

Figure 3-1 Internal block diagram



CW32L010 provides three different packages: QFN20, TSSOP20, SOP16. The functions that can be achieved by products in different packages are different. The details are shown in the following table:

Table 3-1 CW32L010 family device features list

Peripheral		CW32L010F8U6	CW32L010F8P6	CW32L010Y8M6
FLASH（Kbytes）		64		
SRAM（Kbytes）		4		
Timers	Advanced control	1		
	General purpose	1		
	Low-power	1		
	Basic	3		
SPI		1		
I2C		1		
UART		2		
12-bit ADC (number of channels)		1 (14 ext. + 2 int.)		1 (10 ext. + 2 int.)
GPIO		16 + 1(only used for input)		12 + 1(only used for input)
Kernel frequency		48MHz		
Operating voltage		1.62V ~ 5.5V		
Operating temperature		-40°C ~ 85°C		
Package		QFN20	TSSOP20	SOP16

4 Functional overview

4.1 ARM® Cortex®-M0+ core with embedded Flash and SRAM

The ARM® Cortex®-M0+ processor is the latest generation 32-bit core for small embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0+ 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the small memory.

The CW32L010 family has an embedded ARM® core and is therefore compatible with all ARM® tools and software.

4.2 Memories

The device has the following features:

- 4K bytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for high reliability critical applications.
- The non-volatile memory is divided into two arrays:
  - 64K bytes of embedded Flash memory for programs and data
  - 2K bytes of boot program memory
- FLASH memory erasing and reading protection: The FLASH memory erasing and writing protection is performed through the register, and the 4-level read protection level is set through the ISP command.
  - LEVEL0

    No readout protection, the FLASH memory can be read by SWD or ISP.
  - LEVEL1

    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP or SWD interface. After the downgrade, the FLASH is in the whole chip erasing state.
  - LEVEL2

    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP interface. After the downgrade, the FLASH is in the whole chip erasing state.
  - LEVEL3

    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. Protection level downgrade in any way is not supported.

4.3 Boot mode

The CW32L010 supports the following 2 startup modes:

- Boot from the main FLASH memory and run the user program.
- Boot from bootloader memory and run the internal BootLoader.

When running the Bootloader, the user can use the ISP communication protocol for FALSH programming through UART1 (pins are PA07/PA08). The steps for the CW32L010 to enter ISP mode are as follows:

Step 1: Configure the chip in RESET state;

Step 2: Provide a 50kHz square wave to the chip's UART1_RXD (SWDIO);

Step 3: Release the chip's RESET state and delay for 5ms;

Step 4: The chip enters ISP mode.

4.4 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit can generate the CRC code of the data stream according to the selected algorithm and parameter configuration.

In some applications, CRC techniques can be utilized to verify the integrity of data transmission and storage.

The product supports eight commonly used CRC algorithms, including:

CRC16_IBM

CRC16_MAXIM

CRC16_USB

CRC16_MODBUS

CRC16_CCITT

CRC16_CCITT_FALSE

CRC16_X25

CRC16_XMODEM

4.5 Power management

4.5.1 Power supply schemes

- V_{DD} = 1.62V to 5.5V
  Power supply for each digital and analog circuit. Provided externally through VDD pins.

For details about the power supply, refer to *Figure 7-3 Power system*.

4.5.2 Power supply supervisors

The product integrates power-on reset (POR) and brown-out reset (BOR) power monitoring circuits internally, and the power supply is always in an operational state after power-on.The POR/BOR monitors the VDD power supply voltage, and the system enters a reset state when the power supply voltage is monitored to be lower than the reset threshold ($V_{POR/BOR}$). Users do not need to add additional external hardware reset circuit.

4.5.3 Voltage regulator

The internal voltage regulator has "normal" and "low power" operating modes, and it always enabled after reset.

- The "normal" mode corresponds to a state of full speed operation.
- The "low-power" mode corresponds to some power supply working states, including Sleep and DeepSleep working modes.

4.5.4 Low-power modes

The CW32L010 microcontrollers support two low-power modes:

- Sleep mode
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- DeepSleep mode
  DeepSleep is used to achieve the lowest power consumption, the CPU stops running, the high-speed clock modules (HSE, HSIOSC) are automatically turned off, and the low-speed clocks (LSE, LSI) remain unchanged.
  The device exits DeepSleep mode when an external reset, or an IWDT reset, or some peripheral interrupts, or an RTC event occurs.

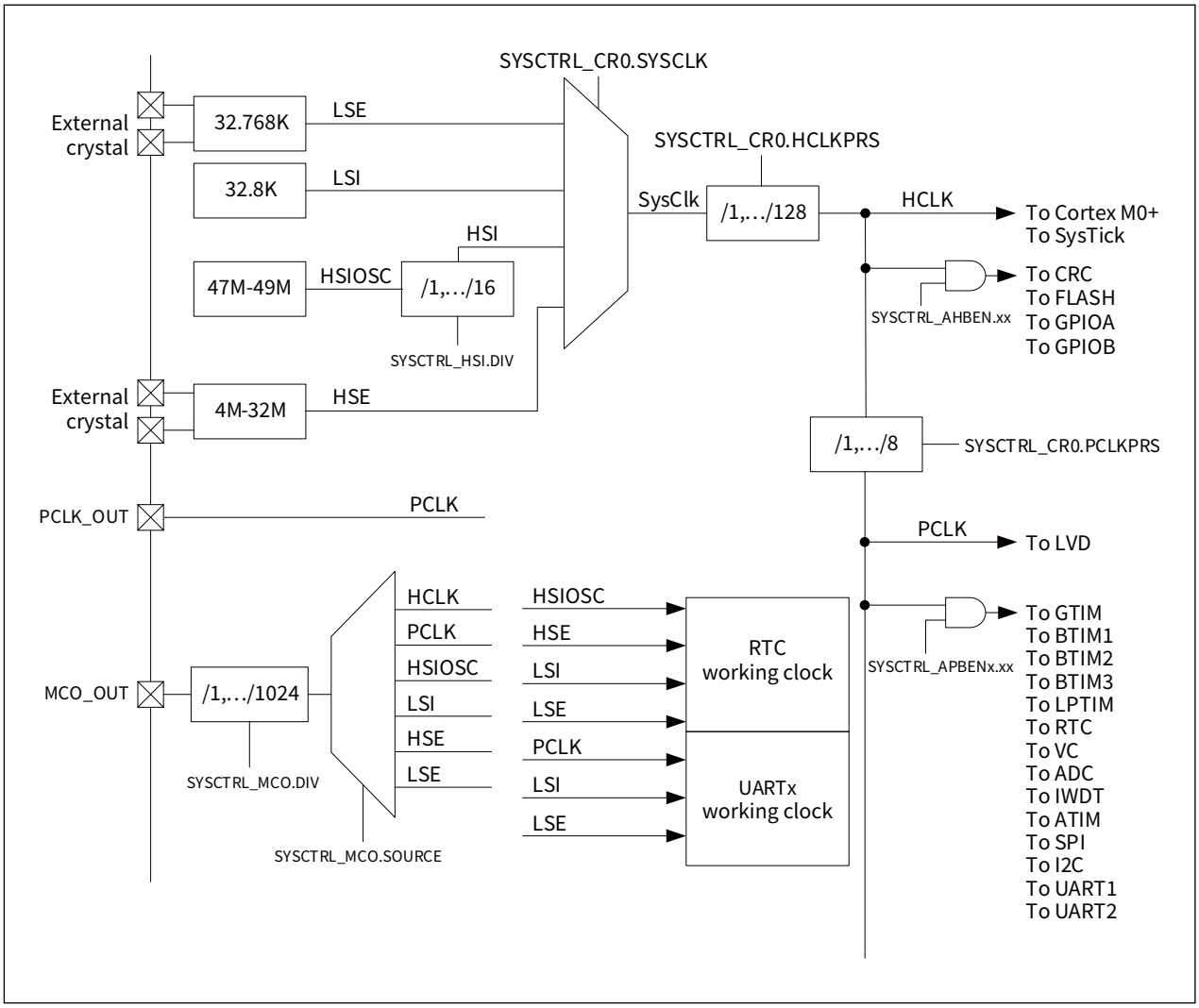
4.6 Clocks and startup

After the MCU is reset, the HSI (generated by the internal 48MHz HSIOSC oscillator frequency division) is selected as the clock source of SysClk by default, and the default value of the system clock frequency is 4MHz. The user can use the program to start the external crystal oscillator and switch the system clock source to the external clock source. The clock failure detection module can continuously detect the state of the external clock source. Once the failure of the external clock source is detected, the system will automatically switch to the internal HSIOSC clock source. If the corresponding fault detection interrupt is enabled, an interrupt will be generated for the user to record fault events.

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

The internal clock tree of the system is shown below :

Figure 4-1 Clock tree of CW32L010



4.7 General-purpose inputs/outputs (GPIO)

Each GPIO pin can be software configured as a push-pull or open-drain digital output, or as a digital input with internal pull-up, as well as peripheral multiplexing. Some GPIO pins have analog functionality and interface with internal analog peripherals. All I/Os can be configured as external interrupt input pins with digital filtering.

4.8 Nested vectored interrupt controller (NVIC)

The CW32L010 family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0+) and supports programmable 4 priority levels.

- Interrupt entry vector table address can be remapped
- Closely coupled NVIC core interface
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved

This hardware block provides flexible interrupt management features with minimal interrupt latency.

4.9 Analog to digital converter (ADC)

The internal 12-bit analog to digital converter has up to 14 external and 2 internal (temperature sensor, BGR 1.2V voltage reference) channels, and support sequence channel conversions mode.

In scan mode, automatic conversion is performed on a selected group of analog inputs.

The analog watchdog function accurately monitors the switching voltage of several selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

4.9.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN14 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of temperature sensor measurement, manufacturers perform individual factory calibrations for each chip. Temperature sensor factory calibration data is stored in FLASH memory.

Table 4-1 Internal temperature sensor calibration value address

ADC reference voltage	Calibration value storage address	Calibration value accuracy
V_{DD}	0x0010 07CE - 0x0010 07CF	±3°C

4.9.2 Internal voltage reference

The nominal output voltage of the built-in BGR module of this chip is 1.2V. The voltage output by BGR module of each chip is slightly different. The voltage output by BGR module has been accurately measured and stored in FLASH when it leaves the factory. The voltage value can be read out by using the expression *((uint16_t*) 0x0010 07D2), and its unit is mV.

4.10 Analog voltage comparator (VC)

Two analog voltage comparators (VC) are integrated inside, which are used to compare two analog input voltages and output the comparison results from the pins. The positive terminal input of the voltage comparator supports up to 4 external analog inputs, and the negative terminal supports not only 2 external analog inputs, but also internal 1.2V voltage reference and internal resistance voltage divider output voltage. The comparison result output has filtering function, hysteresis window function, and polarity selection. Support compare interrupt, which can be used to wake up MCU in low power mode.

The main features of an analog voltage comparator (VC) are:

- Dual analog voltage comparator VC1、VC2
- Internal 8-step resistor divider
- 4 external analog signal inputs
- 2 on-chip analog input signals
  - Built-in Resistor Divider Output Voltage
  - Built-in 1.2V reference voltage
- Selectable output polarity
- Support hysteresis window compare function
- Programmable filters and filter times
- 3 interrupt triggering methods, which can be used in combination
  - High level trigger
  - Rising edge trigger
  - Falling edge trigger
- Support running in low power mode, interrupt wake-up MCU

4.11 Low Voltage Detector (LVD)

Low Voltage Detector (LVD) is used to monitor the VDD power supply voltage or external pin input voltage. When the comparison results between the monitored voltage and the LVD threshold meets the trigger condition, an LVD interrupt or reset signal will be generated, which is usually used to handle some urgent tasks.

The interrupt and reset flags generated by the LVD can only be cleared by software; only after the interrupt or reset flag is cleared and the trigger condition is reached again, the LVD can generate an interrupt or reset signal again.

The main features of a low voltage detector (LVD) are:

- 2-channel monitoring voltage source: VDD power supply voltage, PA03 pin input
- 8-step threshold voltage, range 1.8V~4.6V
- 3 trigger conditions, which can be used in combination
  - Level Triggered: voltage below threshold
  - Falling edge trigger: the falling edge when the voltage falls below the threshold
  - Rising edge trigger: the rising edge when the voltage rises back above the threshold
- Can trigger to generate interrupt or reset signal, both cannot be generated at the same time
- Programmable filter and filter time
- Support hysteresis function
- Support running in low power mode, interrupt wake-up MCU

4.12 Timers and watchdogs

The CW32L010 microcontroller integrates up to 1 general-purpose timer, 3 basic timers, 1 low-power timer and one advanced control timer.

The function differences of timers are shown in the following table:

Table 4-2 Timer feature comparison

Timer type	Timer	Counter bit width	Counter type	Prescaler factor	Capture/ compare channels	Complementary outputs
Advanced control	ATIM	16-bit	Up, down, up/down	1,2,3,4,⋯,65536	6	6
General purpose	GTIM	16-bit	Up, down, up/down	1,2,3,4,⋯,65536	4	0
Low power	LPTIM	16-bit	Up, down, up/down	2^N(N=0,..,7)	2	0
Basic	BTIM1	16-bit	Up	1,2,3,4,⋯,65536	0	1
	BTIM2	16-bit	Up	1,2,3,4,⋯,65536	0	1
	BTIM3	16-bit	Up	1,2,3,4,⋯,65536	0	1

4.12.1 Advanced-control timer (ATIM)

The Advanced-control Timer (ATIM) consists of a 16-bit auto-reload counter, driven by a programmable prescaler. ATIM supports timing, counting, reset, gating, trigger and encoder modes, with 6 independent capture/compare channels, enabling 6 independent PWM outputs or 6 pairs of complementary PWM outputs with dead zones or capture of 6 inputs. Can be used for basic timing/counting, measuring pulse width and period of input signals, generating output waveforms (PWM, single pulse, complementary PWM with dead time inserted, etc.).

4.12.2 General-purpose timer (GTIM)

The general purpose timer (GTIM) contains a 16bit auto-reload counter and is driven by a programmable prescaler.GTIM supports various operating modes such as timing, counting, reset, gating, triggering, and encoder, with 4 independent capture/compare channels to measure the pulse width of the input signals (input capture) or to generate output waveforms (output compare and PWM).

4.12.3 Low-power timer (LPTIM)

The internal integration of a 16-bit low power timer (LPTIM) can realize the function of timing or counting external pulses with very low power consumption. By selecting a suitable clock source and trigger signal, it can realize the function of waking up the system when it sleeps with low power consumption. LPTIM has an internal comparison register, which can realize the comparison output and PWM output, and can control the polarity of the output waveform. In addition, LPTIM can be connected with a quadrature encoder to automatically realize counting up and down.

4.12.4 Basic timers (BTIM1..3)

Three basic timers (BTIMs) are integrated internally, each completely independent and functionally identical, each containing a 16-bit automatic reload counter and driven by a programmable prescaler. BTIM supports four working modes: internal counting mode, external counting mode, trigger startup mode and gated counting mode. It supports interrupt when update event and trigger event occur.Counter reset can be controlled by reset input signal under different working modes.

4.12.5 Independent watchdog (IWDT)

Integrated independent watchdog timer (IWDT), once the IWDT is started, the user needs to reload the counter of the IWDT within a specified time interval, otherwise an overflow will trigger a reset or generate an interrupt signal. After the IWDT is started, the counting can be stopped. The user can choose to keep the IWDT running or suspend counting while in DeepSleep mode.

A specially set key-value register can lock the key registers of the IWDT to prevent the registers from being accidentally modified.

4.12.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features are:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0

4.13 Real-time clock (RTC)

The Real Time Clock (RTC) is a dedicated counter/timer that provides calendar information including hours, minutes, seconds, subseconds, date, month, year, and week day.

RTC has two independent alarm clocks, the time and date can be set in combination, and the alarm clock interrupt can be generated and output through the pin; it supports the time stamp function, which can be triggered by the pin, record the current date and time, and generate a time stamp interrupt at the same time; Support periodic interrupt; support automatic wake-up function, which can generate interrupts and output through pins; support 1Hz square wave and RTCOUT output functions; support internal clock calibration compensation.

The CW32L010 has internal independently calibrated RC clock source with a frequency of 32kHz to provide the drive clock for the RTC. The RTC can run in DeepSleep mode and is suitable for applications requiring low power consumption.

4.14 Inter-integrated circuit interfaces (I2C)

The CW32L010 integrates 1 internal I2C controller, which can serially transmit data to the I2C bus according to the I2C specification at the set transmission rate, and at the same time detect the status during the communication process, and support bus conflict and arbitration processing for multi-master communication.

The main features of the I2C controller are:

- Support master transmit/receive and slave transmit/receive four operating modes
- Support clock stretching (clock synchronization) and multi-master communication conflict arbitration
- Support standard (100Kbps)/fast (400Kbps)/high speed (1Mbps) three operating rates
- Support 7-bit addressing function
- Support 3 slave addresses
- Support broadcast address
- Support input signal noise filtering function
- Support interrupt status query function
- Support SMBUS timeout detection
- Support communication with devices operating at lower voltages than the MCU (via VC)

4.15 Universal asynchronous receiver/transmitter (UART)

Internal integration of 2 universal asynchronous receiver/transmitter (UART), supports asynchronous full-duplex, synchronous half-duplex and single-wire half-duplex modes, supports hardware data flow control and multi-machine communication, also supports LIN (Local Interconnect Network); The data frame structure is programmable, and a wide range of baud rate selection can be provided through the fractional baud rate generator. Built-in timer module supports wait timeout detection, receive idle detection, automatic baud rate detection and general timing functions.

The UART controller works in a dual clock domain, allowing data reception in DeepSleep mode, and the reception completion interrupt can wake the MCU back to Active mode.

Caution: LIN and timer functions are supported for UART1 only; UART2 enables timeout timer related functions by working with slave mode of BTIM/GTIM/ATIM via on-chip peripheral interconnect.

4.16 Serial peripheral interface (SPI)

Serial Peripheral Interface (SPI) supports bidirectional full-duplex, single-wire half-duplex and simplex communication modes, MCU can be configured as master or slave, multi-master communication mode is supported.

The main features of the Serial Peripheral Interface (SPI) are the following:

- Support master mode, slave mode
- Support full-duplex, single-wire half-duplex, simplex
- 4-bit to 16-bit selectable data frame width
- Support transmitting and receiving data LSB or MSB first
- Clock polarity and clock phase is programmable
- Communication rates up to PCLK/2 in master mode
- Support multi-machine communication mode
- 8 interrupt sources with flag bits
- Master mode supports interval frame adjustment
- Transmit buffer empty/receive data complete trigger to start ADC

4.17 Infrared modulation transmitter (IR)

Internal integrated infrared modulation transmitter (IR), through the timer, UART and IRSW soft control bits with the use of a variety of standard PWM or PPM coding can be easily achieved, can also achieve UART data infrared modulation transmission.

The main characteristics of the infrared modulation transmitter (IR) are the following:

- SIR that supports IrDA standard 1.0
- Maximum data rate of 115.2kbps
- IR emitter tube adaptable to high and low levels

4.18 Serial wire debug port (SWD)

An ARM SWD interface is provided, and users can use the CW-DAPLINK of Xinyuan Semiconductor to connect to the MCU to debug and simulate in the IDE development environment.

5 Pin descriptions

Figure 5-1 QFN20 package pinout (top view)

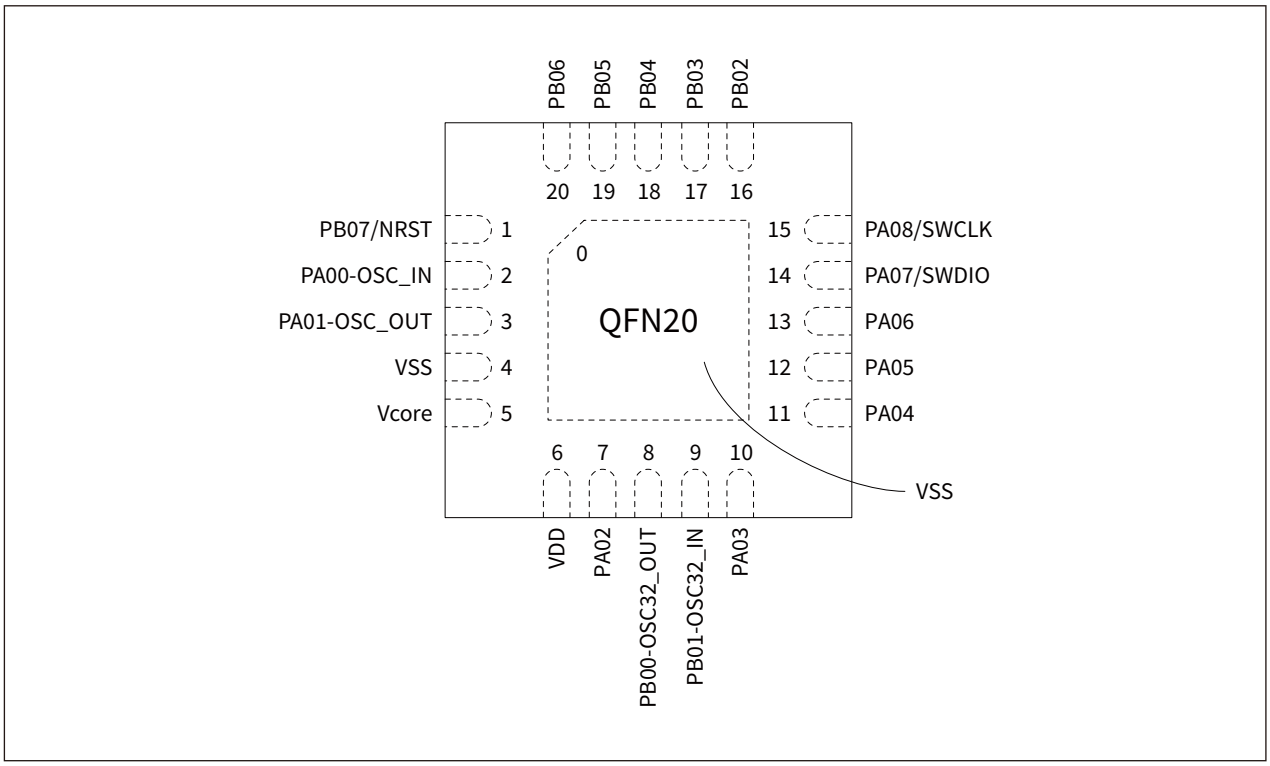


Figure 5-2 TSSOP20 package pinout (top view)

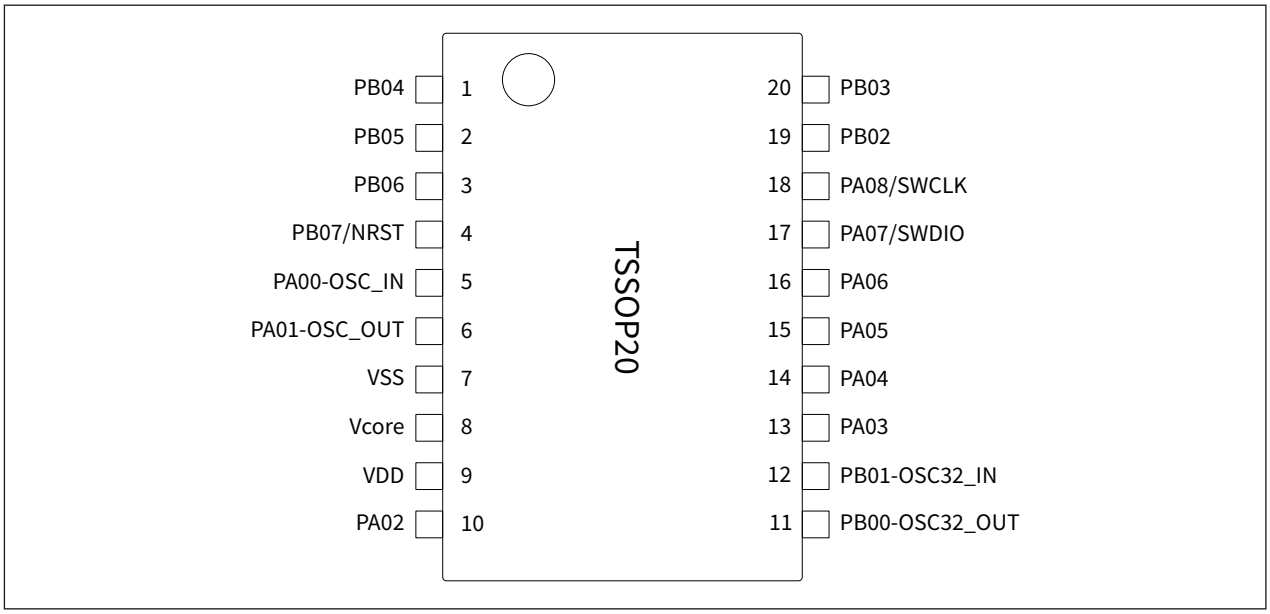


Figure 5-3 SOP16 package pinout (top view)

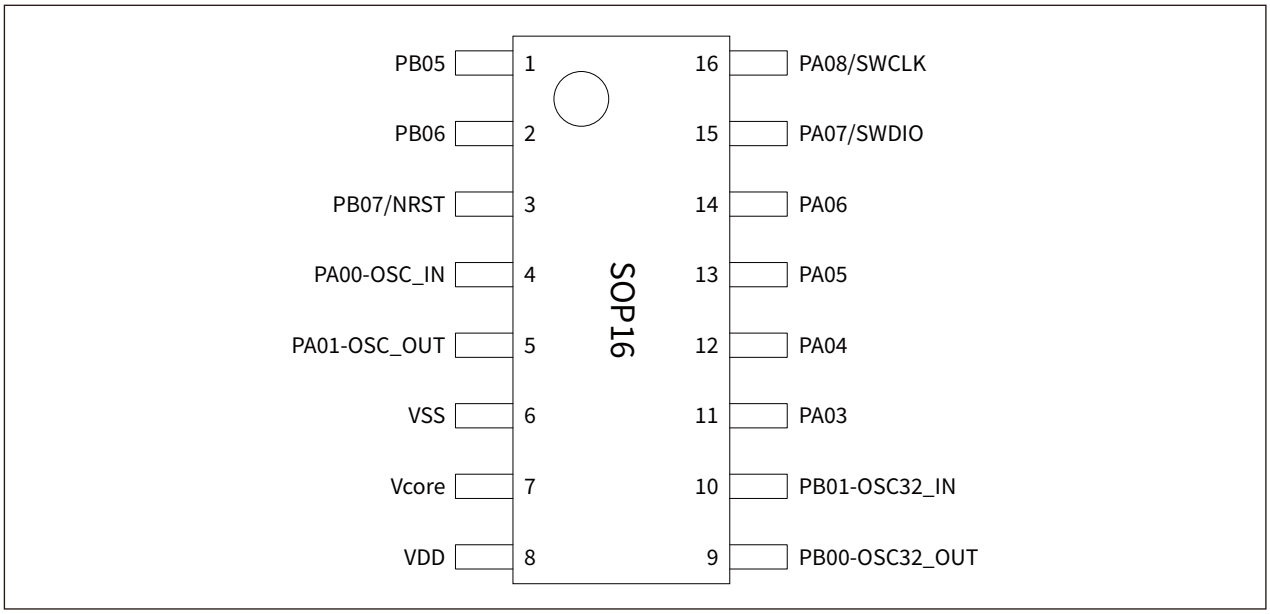


Table 5-1 Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function after reset is the same as the actual pin name.	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/output pin
I/O structure	TTa	Connect the I/O port for the analog function
	TC	Standard I/ O pin
	RST	Reset input pin
Notes	Unless otherwise specified by a note, all pins are set as high impedance input state after reset.	
Additional functions	Digital function	Functions selected through GPIOx_AFRy registers
	Analog function	Functions directly selected through peripheral registers

Table 5-2 CW32L010 pin definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
TSSOP20	QFN20	SOP16					Digital function	Analog function
1	18	-	PB04	I/O	TTa	-	UART2_TXD, RTC_OUT, ADC_SAM, BTIM1_ETR, BTIM2_TOGP, GTIM_CH3, ATIM_CH1	ADC_IN11, VC2_CH3
2	19	1	PB05	I/O	TTa	-	UART2_TXD, RTC_TAMP, SPI_MISO, I2C_SDA, GTIM_ETR, GTIM_CH2, ATIM_CH5	ADC_IN12, VC1_CH0
3	20	2	PB06	I/O	TTa	-	UART2_RXD, RTC_OUT, SPI_MOSI, I2C_SCL, ATIM_ETR, GTIM_CH1, ATIM_CH5N	ADC_IN13, VC2_CH0
4	1	3	PB07/ NRST	I	RST	-	Default is chip reset input, can also be used as GPIO port (only as input), please refer to SYSCTRL_CR2.RSTIO bit field	
5	2	4	PA00	I/O	TTa	-	UART1_RXD, I2C_SDA, SPI_SCK, BTIM1_TOGP, BTIM3_ETR, ATIM_BK2, ATIM_CH4	ADC_IN0, VC1_CH1, OSC_IN
6	3	5	PA01	I/O	TTa	-	UART1_TXD, I2C_SCL, SPI_CS, BTIM1_ TOGN, GTIM_CH3, ATIM_BK, ATIM_CH4N	ADC_IN1, OSC_OUT
7	4	6	VSS	S	-	-	Ground	
8	5	7	Vcore	-	-	-	Vcore is the regulator supply output, must be connected to 1μF capacitor to ground, and only for internal circuit use	
9	6	8	VDD	S	-	-	Power supply	
10	7	-	PA02	I/O	TTa	-	PCLK_OUT, SPI_CS, VC1_OUT, IR_OUT, ATIM_ETR, ATIM_CH1N	ADC_IN2
11	8	9	PB00	I/O	TTa	-	UART1_RXD, UART2_CTS, SPI_SCK, I2C_ SDA, LVD_OUT, BTIM3_TOGP, ATIM_CH1	ADC_IN7, OSC32_OUT
12	9	10	PB01	I/O	TTa	-	UART1_TXD, UART2_RTS, SPI_CS, I2C_ SCL, ADC_SAM, BTIM3_TOGN, ATIM_CH2	ADC_IN8, OSC32_IN
13	10	11	PA03	I/O	TTa	-	UART2_TXD, LPTIM_CH1, SPI_MISO, BTIM1_ETR, IR_OUT, GTIM_CH4, ATIM_ CH3	ADC_IN3, VC1_CH2, LVD_CH1
14	11	12	PA04	I/O	TTa	-	UART2_RXD, LPTIM_CH2, SPI_MOSI, MCO_OUT, VC2_OUT, GTIM_CH3, ATIM_CH1N	ADC_IN4
15	12	13	PA05	I/O	TTa	-	UART1_RXD, LPTIM_OUT, SPI_SCK, I2C_ SDA, HEXEN, GTIM_CH2, ATIM_CH2N	ADC_IN5, VC2_CH1
16	13	14	PA06	I/O	TTa	-	UART1_TXD, LPTIM_ETR, SPI_MOSI, I2C_ SCL, BTIM2_ETR, GTIM_CH1, ATIM_CH3N	ADC_IN6

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
TSSOP20	QFN20	SOP16					Digital function	Analog function
17	14	15	PA07/ SWDIO	I/O	TC	1	UART1_RXD, I2C_SDA, SPI_MISO, LPTIM_OUT, BTIM2_TOGP, ATIM_BK, ATIM_CH6	
18	15	16	PA08/ SWCLK	I/O	TC	1	UART1_TXD, I2C_SCL, MCO_OUT, VC1_OUT, BTIM2_TOGN, ATIM_BK2, ATIM_CH6N	
19	16	-	PB02	I/O	TTa	-	UART2_TXD, UART1_CTS, SPI_MISO, VC2_OUT, LPTIM_CH1, GTIM_ETR, ATIM_CH2	ADC_IN9, VC2_CH2
20	17	-	PB03	I/O	TTa	-	UART2_RXD, UART1_RTS, SPI_MOSI, MCO_OUT, BTIM2_TOGN, GTIM_CH4, ATIM_CH2N	ADC_IN10, VC1_CH3

Caution 1: Afeter reset，these pins are configured as SWDIO and SWCLK functions，and the internal pull-up resistors are turned on by default.

Table 5-3 Alternate functions selected through GPIOA_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA00	UART1_RXD	I2C_SDA	SPI_SCK	BTIM1_TOGP	BTIM3_ETR	ATIM_BK2	ATIM_CH4
PA01	UART1_TXD	I2C_SCL	SPI_CS	BTIM1_TOGN	GTIM_CH3	ATIM_BK	ATIM_CH4N
PA02	PCLK_OUT		SPI_CS	VC1_OUT	IR_OUT	ATIM_ETR	ATIM_CH1N
PA03	UART2_TXD	LPTIM_CH1	SPI_MISO	BTIM1_ETR	IR_OUT	GTIM_CH4	ATIM_CH3
PA04	UART2_RXD	LPTIM_CH2	SPI_MOSI	MCO_OUT	VC2_OUT	GTIM_CH3	ATIM_CH1N
PA05	UART1_RXD	LPTIM_OUT	SPI_SCK	I2C_SDA	HEXEN	GTIM_CH2	ATIM_CH2N
PA06	UART1_TXD	LPTIM_ETR	SPI_MOSI	I2C_SCL	BTIM2_ETR	GTIM_CH1	ATIM_CH3N
PA07	UART1_RXD	I2C_SDA	SPI_MISO	LPTIM_OUT	BTIM2_TOGP	ATIM_BK	ATIM_CH6
PA08	UART1_TXD	I2C_SCL	MCO_OUT	VC1_OUT	BTIM2_TOGN	ATIM_BK2	ATIM_CH6N

Table 5-4 Alternate functions selected through GPIOB_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB00	UART1_RXD	UART2_CTS	SPI_SCK	I2C_SDA	LVD_OUT	BTIM3_TOGP	ATIM_CH1
PB01	UART1_TXD	UART2_RTS	SPI_CS	I2C_SCL	ADC_SAM	BTIM3_TOGN	ATIM_CH2
PB02	UART2_TXD	UART1_CTS	SPI_MISO	VC2_OUT	LPTIM_CH1	GTIM_ETR	ATIM_CH2
PB03	UART2_RXD	UART1_RTS	SPI_MOSI	MCO_OUT	BTIM2_TOGN	GTIM_CH4	ATIM_CH2N
PB04	UART2_TXD	RTC_OUT	ADC_SAM	BTIM1_ETR	BTIM2_TOGP	GTIM_CH3	ATIM_CH1
PB05	UART2_TXD	RTC_TAMP	SPI_MISO	I2C_SDA	GTIM_ETR	GTIM_CH2	ATIM_CH5
PB06	UART2_RXD	RTC_OUT	SPI_MOSI	I2C_SCL	ATIM_ETR	GTIM_CH1	ATIM_CH5N

6 Address mapping

Figure 6-1 CW32L010 internal address mapping

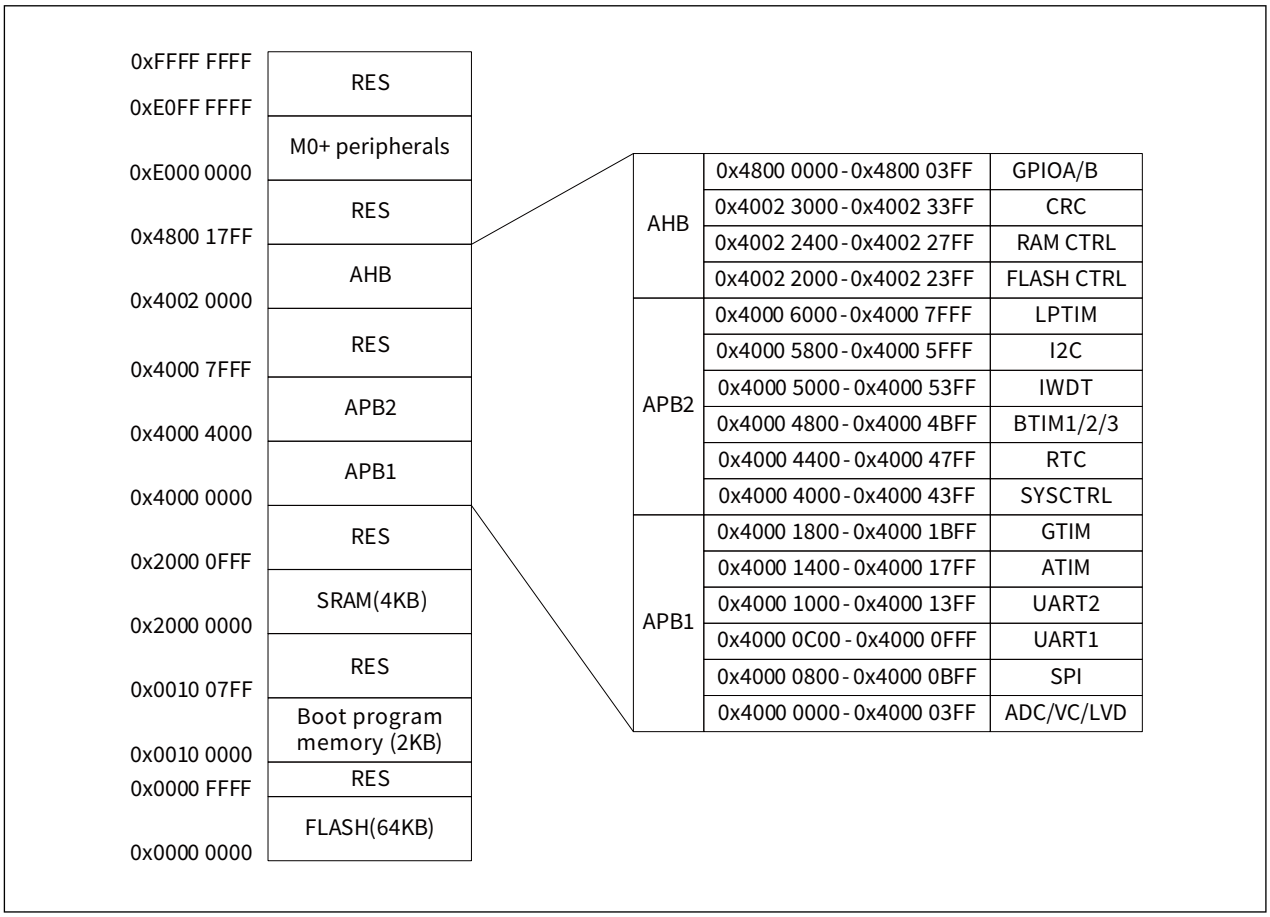


Table 6-1 CW32L010 peripheral register boundary addresses

Device or bus	Boundary address	Size	Peripheral
Main FLASH memory	0x0000 0000 - 0x0000 FFFF	64KB	Main FLASH
Boot program memory	0x0010 0000 - 0x0010 07FF	2KB	BootLoader
OTP memory	0x0010 0760 - 0x0010 0775	22B	OTP
SRAM memory	0x2000 0000 - 0x2000 0FFF	4KB	SRAM
APB1 peripheral	0x4000 0000 - 0x4000 03FF	1KB	ADC/VC/LVD
	0x4000 0800 - 0x4000 0BFF	1KB	SPI
	0x4000 0C00 - 0x4000 0FFF	1KB	UART1
	0x4000 1000 - 0x4000 13FF	1KB	UART2
	0x4000 1400 - 0x4000 17FF	1KB	ATIM
	0x4000 1800 - 0x4000 1BFF	1KB	GTIM
APB2 peripheral	0x4000 4000 - 0x4000 43FF	1KB	SYSCTRL
	0x4000 4400 - 0x4000 47FF	1KB	RTC
	0x4000 4800 - 0x4000 4BFF	1KB	BTIM123
	0x4000 5000 - 0x4000 53FF	1KB	IWDT
	0x4000 5800 - 0x4000 5FFF	1KB	I2C
	0x4000 6000 - 0x4000 7FFF	1KB	LPTIM
AHB peripheral	0x4002 2000 - 0x4002 23FF	1KB	FLASH CTRL
	0x4002 2400 - 0x4002 27FF	1KB	RAM CTRL
	0x4002 3000 - 0x4002 33FF	1KB	CRC
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA/B
M0+ peripheral	0xE000 0000 - 0xE00F FFFF	1MB	M0+ peripheral

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3Σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C and V_{DD} = 3.3V. They are given only as design guidelines and are not tested.

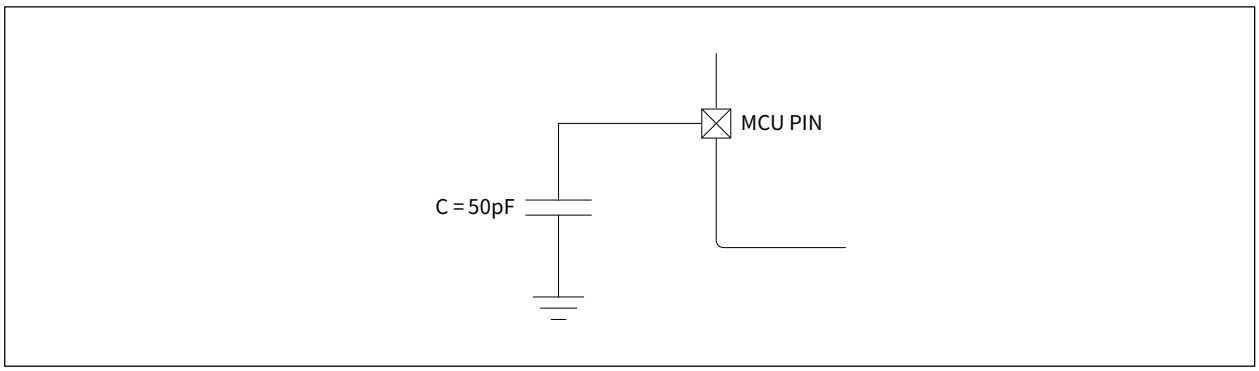
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below:

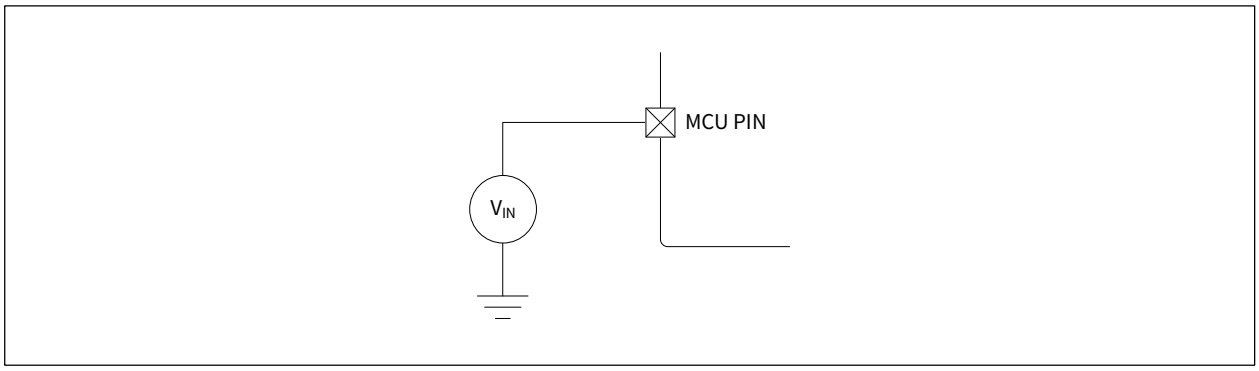
Figure 7-1 Pin loading conditions



7.1.5 Pin input voltage

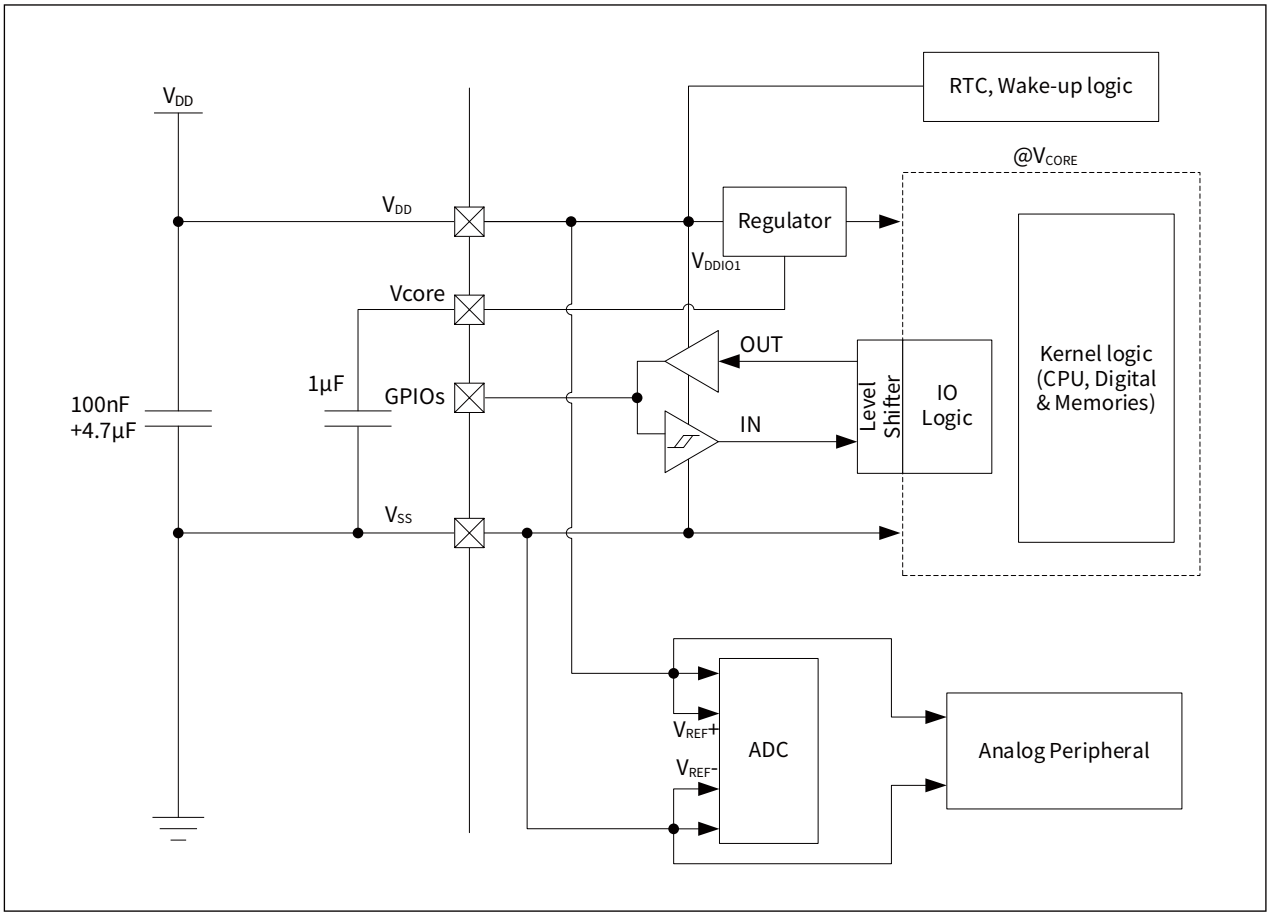
The input voltage measurement on a pin of the device is described in the figure below:

Figure 7-2 Pin input voltage



7.1.6 Power system

Figure 7-3 Power system



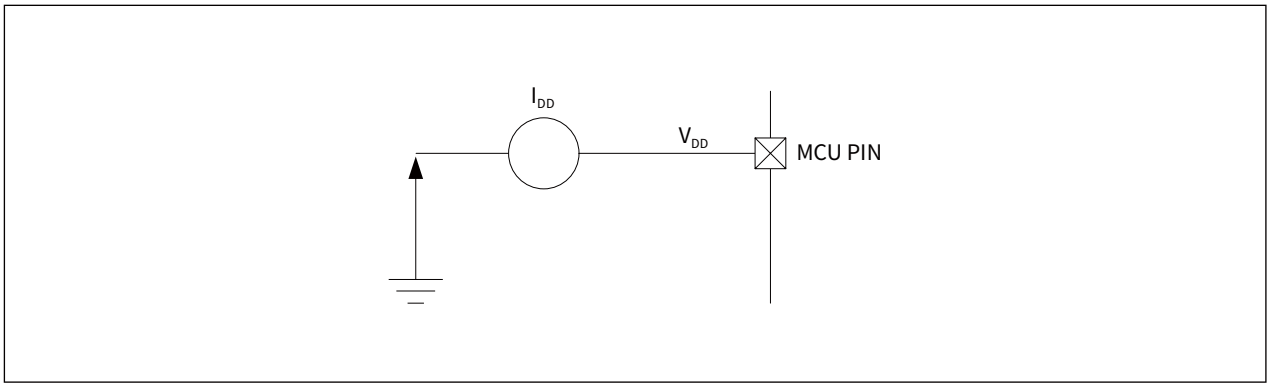
Caution 1: Each power supply pair (V_{DD}/V_{SS}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Caution 2: All V_{DD} pins must be powered and at the same voltage.

Caution 3: Vcore is the regulator supply output and must be connected to a 1µF capacitor to ground and is for internal circuit use only.

7.1.7 Current consumption measurement

Figure 7-4 Method of measurement



7.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 7-1, Table 7-2 and Table 7-3 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7-1 Voltage characteristics[1]

Symbol	Ratings	Min.	Max.	Unit
V_{DD} - V_{SS}	External main supply voltage	-0.3	6.0	V
V_{IN}[2]	Input voltage on port IO	V_{SS} - 0.3	V_{DD} + 0.3	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	*See Table 7-22 ESD & LU characteristics*		kV

Caution 1: All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply, in the permitted range.

Caution 2: V_{IN} maximum must always be respected，refer to Table 7-2 for the maximum allowable injection current value.

Table 7-2 Current characteristics

Symbol	Ratings	Max.	Unit
$I_{VDD(PIN)}$	Total current into sum of a single V_{DD} power lines (source) [1]	+100	mA
$I_{VSS(PIN)}$	Total current out of sum of a single V_{SS} power lines (sink) [1]	-100	
$I_{IO(PIN)}$	Current into a single I/O or control pin	+25	
	Current out of a single I/O or control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os or control pins	+80	
	Total output current sourced by sum of all I/Os or control pins	-80	
$I_{INJ(PIN)}$[2、3]	Injected current on TC and RST pins	±5	
	Injected current on TTa pins	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) [4]	±25	

Caution 1: All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply, in the permitted range.

Caution 2: $I_{INJ(PIN)}$ must not exceed its limit to ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed to not to exceed its maximum value, also ensure that external limit $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.

Caution 3: Negative injection disturbs the analog performance of the device.

Caution 4: When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents. This result is based on the characterization of the maximum value of $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	105	

7.3 Operating conditions

7.3.1 General operating conditions

Table 7-4 General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB bus frequency	$V_{DD} \geqslant 1.8V$	0	48	MHz
f_{PCLK}	Internal APB bus frequency	$V_{DD} \geqslant 1.8V$	0	48	
f_{HCLK}	Internal AHB bus frequency	$1.62V \leqslant V_{DD} < 1.8V$	0	24	
f_{PCLK}	Internal APB bus frequency	$1.62V \leqslant V_{DD} < 1.8V$	0	24	
V_{DD}	Standard operating voltage	-	1.62	5.5	V
V_{IN}	I/O input voltage	TC I/O	-0.3	V_{DD} + 0.3	V
		TTa I/O	-0.3	V_{DD} + 0.3	
P_D	Power dissipation at T_A = 85°C for suffix 6 [1]	TSSOP20	-	263	mW
		QFN20	-	220	
		SOP16	-	500	
T_A	Ambient temperature (suffix 6 version)	Maximum power dissipation	-40	85	°C
		Low power dissipation [2]	-40	105	
T_J	Junction temperature range	Suffix 6 version	-40	105	°C

Caution 1: If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (See 8.7 Thermal characteristics).

Caution 2: In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (See 8.7 Thermal characteristics).

7.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are tested under the working conditions listed in *Table 7-4 General operating conditions*.

Table 7-5 Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0	10000	μs/V
	V_{DD} fall time rate		20	10000	

7.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are tested under the working conditions listed in *Table 7-4 General operating conditions*.

Table 7-6 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{POR/BOR}$	Power on/brown-out reset threshold	Falling edge	1.45 [1]	1.50	1.55 [2]	V
		Rising edge	1.50 [2]	1.55	1.60	V
$V_{BORhyst}$ [3]	BOR hysteresis	-	-	50	-	mV
$t_{RSTTEMPO}$ [3]	Reset temporization	-	4	6.5	18	ms

Caution 1: The product behavior is guaranteed by design down to the minimum $V_{POR/BOR}$ value.

Caution 2: Data based on characterization results, not tested in production.

Caution 3: Guaranteed by design, not tested in production.

7.3.4 Internal reference voltage

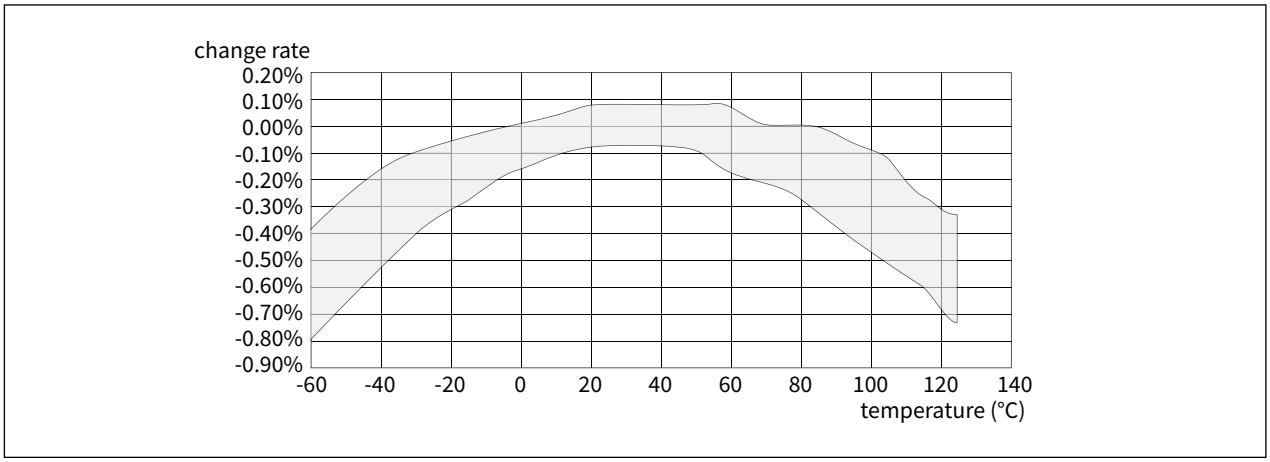
Table 7-7 Internal reference voltage

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{REFINT1V2}$	Internal 1.2V reference voltage	-40°C < T_A < +85°C	-	1.2[2]	-	V
T_{Coeff} [1]	Temperature coefficient	-	-40	-	+40	ppm/°C
t_{setup}	Set-up time	-	-	45	-	µs

Caution 1: Guaranteed by design, not tested in production. The range of measured voltage data change rate of multiple chips is shown in the shaded part of the figure below.

Caution 2: The actual value of the internal 1.2V reference voltage of each chip is stored in FLASH, see ADC chapter of 'user manual' for details.

Figure 7-5 BGR 1.2V output voltage temperature characteristics



7.3.5 Supply current characteristics

Current consumption is affected by many factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

Figure 7-4 Method of measurement shows the circuit for testing current consumption.

All result of the Run-mode current consumption measurements based on the same limited code used to test CoreMark.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency :
  - 0 wait state inserted when 0 to 24MHz
  - 1 wait state inserted when above 24MHz
  - 2 wait state inserted when above 48MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The data given in Table 7-8 to Table 7-11 are derived from tests performed under the ambient temperature and supply voltage noted in the remarks. For the test conditions, see *Table 7-4 General operating conditions*。

Table 7-8 Typical and maximum current consumption

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled		All peripherals disabled		Unit
				Typ.	Max.[1] T_A = 85°C	Typ.	Max.[1] T_A = 85°C	
I_{DD}	Supply current in Active mode, (code executing from Flash)	HSI or HSE clock	48MHz	4.22	4.6	2.7	3.1	mA
			24MHz	2.8	3.2	2.1	2.4	
			12MHz	1.87	2.1	1.45	1.69	
			8MHz	1.58	1.69	1.29	1.42	
			4MHz	1.12	1.30	1.0	1.16	
I_{DD}	Supply current in Active mode (code executing from RAM)	HSI or HSE clock	48MHz	4.18	4.3	2.55	2.64	
			24MHz	2.28	2.36	1.48	1.55	
			8MHz	1.02	1.08	0.76	0.81	
			4MHz	0.71	0.75	0.58	0.62	
I_{DD}	Supply current in Sleep mode (code executing from Flash or RAM)	HSI or HSE clock	48MHz	2.51	2.59	0.92	0.96	
			24MHz	1.47	1.53	0.66	0.7	
			8MHz	0.76	0.8	0.48	0.55	
			4MHz	0.57	0.62	0.44	0.49	

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.

Table 7-9 Current consumption when system clock is LSE

Symbol	Parameter	Conditions		V_{DD} = 1.62V~5.5V		V_{DD} = 3.3V	Unit
				Min.[1]	Max.[1]	Typ.	
I_{DD}	Supply current in Active mode (code executing from FLASH, all peripheral clocks enabled)	LSE=32768Hz (DRIVER=0)	T_A = -40°C	68	84	75	μA
			T_A = 25°C	71	85	76	
			T_A = 50°C	73	90	78	
			T_A = 85°C	78	102	85	
	Supply current in Active mode (code executing from FLASH, all peripheral clocks disabled)	LSE=32768Hz (DRIVER=0)	T_A = -40°C	67	83	73	
			T_A = 25°C	70	84	75	
			T_A = 50°C	72	89	77	
			T_A = 85°C	77	101	84	

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.

Table 7-10 Typical and maximum current consumption in DeepSleep

Symbol	Parameter	Conditions	Typ. @V_{DD}	Max.[1]	Unit
			3.3V	T_A=85°C	
I_{DD}	Supply current in DeepSleep mode	The regulator is in Active mode, all oscillators are off	0.3	1.5	μA
		The regulator is in Active mode, LSE, RTC and IWDT are on	1.23	2.63	

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = 3.3V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency:
  - 0 wait state inserted when 0 to 24MHz
  - 1 wait state inserted when above 24MHz
  - 2 wait state inserted when above 48MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$

Table 7-11 Typical current consumption in Active mode, program running from FLASH

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Active mode	Runs from FLASH with 48MHz internal HSIOSC clock	48MHz	4.22	2.7	mA
			24MHz	2.8	2.1	
			12MHz	1.87	1.45	
			8MHz	1.58	1.29	
			4MHz	1.12	1.0	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

- I/O static current consumption

  All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up resistors values given in *Table 7-23 I/O static characteristics*.

  For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

  If the input voltage level of the I/Os is the intermediate voltage level, it will continuously cause the internal Schmitt trigger to flip, resulting in additional random current consumption (although it is small). If it is required to judge the level flip situation in real time, that should configure the I/Os in analog input mode to avoid this.

Caution 1: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

- I/O dynamic current consumption

  In addition to the internal peripheral current consumption measured previously, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

  $$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

  where:

  I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load.

  V_{DDIOx} is the I/O supply voltage.

  f_{SW} is the I/O switching frequency.

  C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

  C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 7-12 Switching output I/O current consumption

Symbol	Parameter	Conditions [1]	I/O toggling frequency (f_{SW})	Typ.	Unit
I_{SW}	I/O current consumption	V_{DDIOx} = 3.3V C_{EXT} = 0pF $C = C_{INT} + C_{EXT} + C_S$	4MHz	0.18	mA
			8MHz	0.37	
			16MHz	0.76	
			24MHz	1.39	
		V_{DDIOx} = 3.3V C_{EXT} = 22pF $C = C_{INT} + C_{EXT} + C_S$	4MHz	0.49	
			8MHz	0.94	
			16MHz	2.38	
			24MHz	3.99	
		V_{DDIOx} = 3.3V C_{EXT}= 47pF $C = C_{INT} + C_{EXT} + C_S$	4MHz	0.81	
			8MHz	1.7	
			16MHz	3.67	

Caution 1: C_S = 7pF (estimated value).

7.3.6 Wakeup time from low-power mode

The wakeup times given in the table below are tested during the wake-up phase of the HSIOSC.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode and DeepSleep mode.

All test environments are from ambient temperature and supply voltage conditions summarized in *Table 7-4 General operating conditions*.

Table 7-13 Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ. @V_{DD}	Max.	Unit
			3.3V		
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4	-	HCLK
t_{WUDEEP}	Wakeup form DeepSleep mode	Regulator in Active mode	5.5	6.5	μs

7.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

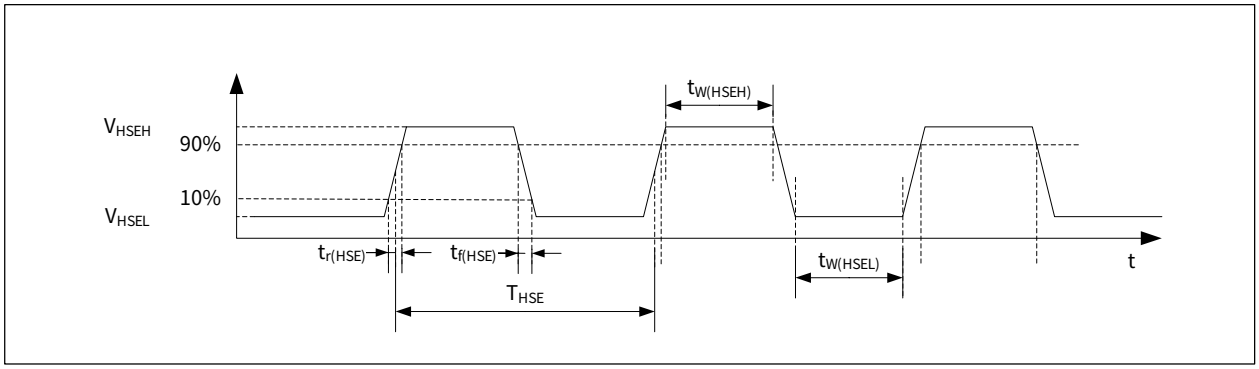
The external clock signal has to respect the I/O characteristics in section *7.3.11 I/O port characteristics.* The recommended clock input waveform is shown in *Figure 7-6 High-speed external clock source AC timing diagram*.

Table 7-14 High-speed external clock input characteristics

Symbol	Parameter [1]	Min.	Typ.	Max.	Unit
f_{HSE_EXT}	User external clock source frequency	1	-	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

Caution 1: Guaranteed by design, not tested in production.

Figure 7-6 High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

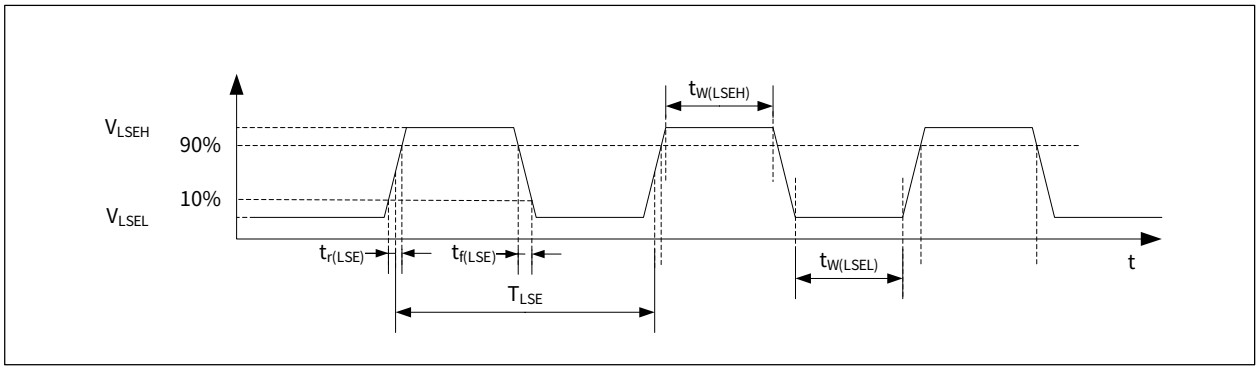
The external clock signal has to respect the I/O characteristics in section *7.3.11 I/O port characteristics.* The recommended clock input waveform is shown in *Figure 7-7 Low-speed external clock source AC timing diagram*.

Table 7-15 Low-speed external clock input characteristics

Symbol	Parameter [1]	Min.	Typ.	Max.	Unit
f_{LSE_EXT}	User external clock source frequency	-	32.768	100	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{W(LSEH)}$ $t_{W(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

Caution 1: Guaranteed by design, not tested in production.

Figure 7-7 Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4MHz~32MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 7-16 HSE oscillator characteristics

Symbol	Parameter	Conditions [1]	Min. [2]	Typ.	Max. [2]	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
R_F	Feedback resistor	-	-	330	-	kΩ
I_{DD}	HSE current consumption	During startup [3]	-	-	700	μA
		V_{DD}= 3.3 V, R_m = 45 Ω, C_L = 10 pF@8 MHz	-	360	-	
		V_{DD} = 3.3 V, R_m = 30 Ω, C_L = 20 pF@32 MHz	-	500	-	
$t_{su(HSE)}$ [4]	Startup time	V_{DD} is stabilized	-	2	-	ms

Caution 1: Resonator characteristics given by the crystal/ceramic resonator manufacturer.

Caution 2: Guaranteed by design, not tested in production.

Caution 3: This consumption level occurs during the first 2/3 of the $t_{su(HSE)}$ startup time.

Caution 4: $t_{su(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 7-17 LSE oscillator characteristics (f_{LSE} = 32.768kHz)

Symbol	Parameter [1]	Conditions	Min. [1]	Typ.	Max. [1]	Unit
I_{DD}	LSE current consumption	DRIVER=0	-	0.3	-	μA
		DRIVER=1	-	0.33	-	
		DRIVER=2	-	0.37	-	
		DRIVER=3	-	0.41	-	
		DRIVER=4	-	0.45	-	
		DRIVER=5	-	0.49	-	
		DRIVER=6	-	0.53	-	
		DRIVER=7	-	0.56	-	
		DRIVER=8	-	1.34	-	
		DRIVER=9	-	1.38	-	
		DRIVER=10	-	1.42	-	
		DRIVER=11	-	1.46	-	
		DRIVER=12	-	1.50	-	
		DRIVER=13	-	1.54	-	
		DRIVER=14	-	1.57	-	
		DRIVER=15	-	1.61	-	
$t_{su(LSE)}$ [2]	Startup time	V_{DD} is stabilized	-	1.50	-	s

Caution 1: Guaranteed by design, not tested in production.

Caution 2: $t_{su(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

7.3.8 Internal clock source characteristics

The data given in the following table is based on the sample tests of the test environment indicated by *Table 7-4 General operating conditions*.

High-speed internal (HSIOSC) RC oscillator

Table 7-18 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
TRIM	HSI user trimming step	-	-	0.2	-	%
$Duty_{HSI}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = -40°C ~ +85°C	-2.0	-	+2.0	%
		T_A = -20°C ~ +50°C	-1.0	-	+1.0	%
		T_A = +25°C	-0.5	-	+0.5	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	5.5	-	6	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	300	-	μA

Low-speed internal (LSI) RC oscillator

Table 7-19 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	-	32.8	-	kHz
TRIM	LSI user trimming step	-	-	0.16	-	%
$Duty_{LSI}$	Duty cycle	-	30	-	70	%
ACC_{LSI}	Accuracy of the LSI oscillator (factory calibrated)	T_A = -40°C ~ +85°C	-3	-	+3	%
		T_A = +25°C	-1	-	+1	%
$t_{SU(LSI)}$	LSI oscillator startup time	-	-	-	50	μs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	1	-	μA

7.3.9 Memory characteristics

FLASH memory

The characteristics are for 40°C to +85°C test enviroment unless otherwise specified.

Table 7-20 FLASH memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max. [1]	Unit
t_{prog8}	8-bit programming time	T_A = -40°C ~ +85°C	-	31	-	μs
t_{prog16}	16-bit programming time	T_A = -40°C ~ +85°C	-	39	-	μs
t_{prog32}	32-bit programming time	T_A = -40°C ~ +85°C	-	55	-	μs
t_{ERASE}	Page erase time	T_A = -40°C ~ +85°C	-	2.5	-	ms
t_{ME}	Mass erase time	T_A = -40°C ~ +85°C	-	35	-	ms
I_{DD}	Supply current	Write mode	-	-	2	mA
		Erase mode	-	-	1	mA

Caution 1: Guaranteed by design, not tested in production.

Table 7-21 FLASH memory endurance and data retention

Symbol	Parameter	Conditions	Min. [1]	Unit
N_{NED}	Endurance	T_A = -40°C ~ +85°C	10	k times
t_{RET}	Data retention	T_A = -40°C ~ +85°C	25	Years

Caution 1: Obtained by comprehensive evaluation, not tested in production.

7.3.10 ESD & LU characteristics

Use specific measurement methods to test the strength of the chip to determine its electrical sensitivity performance.

Table 7-22 ESD & LU characteristics

Symbol	Parameter	Condition	Typ.	Max.	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JS-001: 2023	-	±6	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JS-002: 2022	-	±2	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A = +25 °C, conforming to JESD22-A115C: 2010	-	±200	V
LU	Static Latch-Up	T_A = +85 °C, conforming to JESD78F: 2022	-	±600	mA

7.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-23 I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	0.3 V_{DDIOx}	V
V_{IH}	High level input voltage	TC and TTa I/O	0.7 V_{DDIOx}	-	-	V
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	450 [1]	-	mV
I_{ikg}	Input leakage current	TC and TTa I/O in digital mode $V_{SS} \leqslant V_{IN} \leqslant V_{DD}$	-	-	±0.1	µA
		TTa I/O in analog mode $V_{SS} \leqslant V_{IN} \leqslant V_{DD}$	-	-	±0.2	
R_{PU} [2]	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	55	-	70	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Caution 1: Data based on design simulation only. Not tested in production.

Caution 2: Pull-up resistors is designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal.

Output driving current

The GPIOs can sink or source up to ±8mA, and sink or source up to ±20mA with a relaxed V_{OH} and V_{OL}.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in section *7.2 Absolute maximum ratings*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 7-1 Voltage characteristics*[1]).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 7-1 Voltage characteristics*[1]).

Output voltage levels

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-24 Output voltage characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	High-level output voltage source current	Sourcing 10mA, V_{DD} = 3.3V[1]	2.95	-	V
		Sourcing 20mA, V_{DD} = 3.3V[2]	2.7	-	
V_{OL}	Low-level output voltage sink current	Sinking 10mA, V_{DD} = 3.3V[1]	-	0.28	
		Sinking 20mA, V_{DD} = 3.3V[2]	-	0.60	

Caution 1: The maximum total current I_{OH}(max) and I_{OL}(max) of all output combinations should not exceed 40mA to meet the maximum specified voltage drop.

Caution 2: The maximum total current I_{OH}(max) and I_{OL}(max) of all output combinations should not exceed 100mA to meet the maximum specified voltage drop.

Input/output AC characteristics

The values and definitions of the AC characteristics of the I/Os are given by the following charts respectively.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

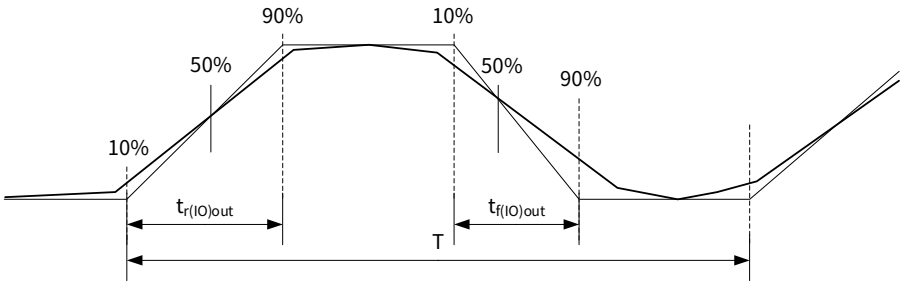
Table 7-25 I/O AC characteristics

Symbol	Parameter	Conditions	Min	Max[1]	Unit
$f_{max(IO)out}$	Maximum frequency [2]	C_L = 30pF，$V_{DDIOx} \geqslant$ 2.7V	-	50	MHz
		C_L = 50pF，$V_{DDIOx} \geqslant$ 2.7V	-	30	
		C_L = 50pF，2.4V $\leqslant V_{DDIOx} <$ 2.7V	-	20	
$t_{f(IO)out}$	Output fall time	C_L = 30pF，$V_{DDIOx} \geqslant$ 2.7V	-	5	ns
		C_L = 50pF，$V_{DDIOx} \geqslant$ 2.7V	-	8	
		C_L = 50pF，2.4V $\leqslant V_{DDIOx} <$ 2.7V	-	12	
$t_{r(IO)out}$	Output rise time	C_L = 30pF，$V_{DDIOx} \geqslant$ 2.7V	-	5	
		C_L = 50pF，$V_{DDIOx} \geqslant$ 2.7V	-	8	
		C_L = 50pF，2.4V $\leqslant V_{DDIOx} <$ 2.7V	-	12	

Caution 1: Data based on design simulation only. Not tested in production.

Caution 2: The maximum frequency is defined in the figure below.

Figure 7-8 I/O AC characteristics definition



Maximum frequency is achieved if ($t_r + t_f$) $\leqslant$ 2/3T and if the duty cycle is (45-55%) when loaded by C_L

7.3.12 NRST pin characteristics

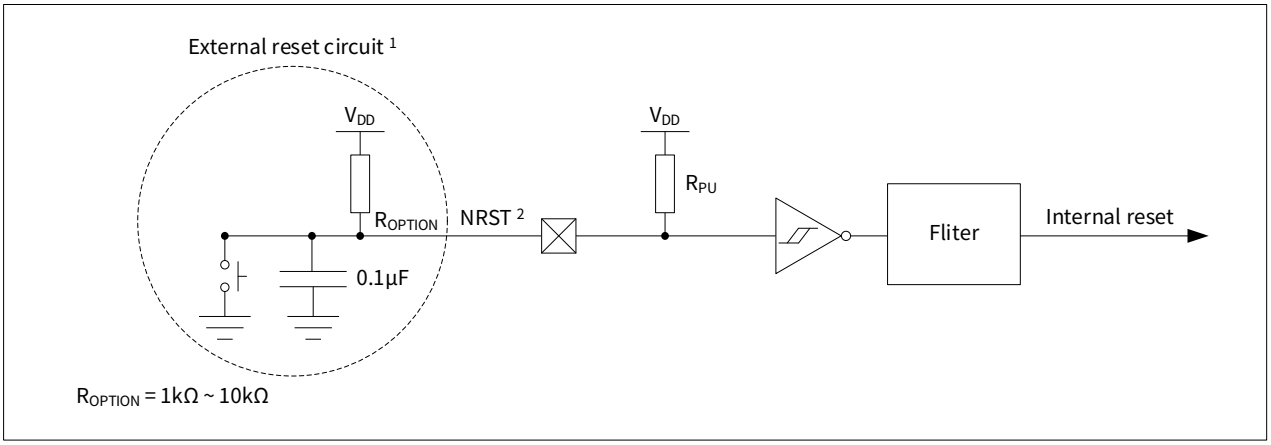
The NRST pin is connected to a permanent pull-up resistor R_{PU} internally.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

Table 7-26 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3V_{DD}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7V_{DD}$	-	-	-
$V_{hys(NRST)}$	NRST input voltage hysteresis	-	-	300	-	mV
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	-	7	-	kΩ
$V_{F(NRST)}$	Minimum required reset pulse width	-	20	-	-	μs

Figure 7-9 Recommended NRST pin protection



Caution 1: The external capacitor protects the device against parasitic resets.

Caution 2: The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 7-26 NRST pin characteristics. Otherwise the reset will not be taken into account by the device.

7.3.13 12-bit ADC characteristics

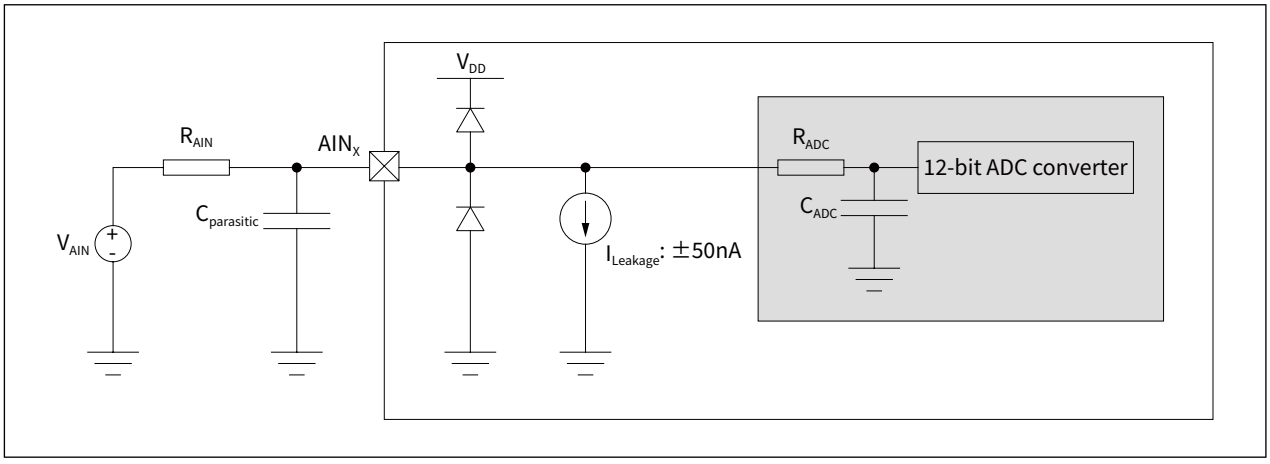
Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions.*

Table 7-27 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage for ADC ON	-	1.62	-	5.5	V
$I_{DD(ADC)}$	Current consumption of the ADC	V_{DD} = 3.3V	-	300	-	μA
f_{ADC}	ADC clock frequency	-	-	48	-	MHz
f_S	Sampling rate	-	-	-	2	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 48MHz	-	-	1.6	MHz
V_{AIN}	Conversion voltage range	-	0	-	V_{DD}	V
R_{AIN}	External input impedance	-	See *Table 7-28 Maximum input impedance table*			kΩ
R_{ADC}	Sampling switch resistor	-	-	1.8	-	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	4	-	pF
t_S	Sampling time	1.62V < V_{DD} < 1.8V	1.25	-	-	μs
		1.8V < V_{DD} < 2.8V	0.75	-	-	
		2.8V < V_{DD} < 3.3V	0.375	-	-	
		3.3V < V_{DD} < 5.5V	0.1875	-	-	
t_{STAB}	Stabilization time	-	15			1 / f_{ADC}
t_{CONV}	Total conversion time (including sampling time)	-	21	-	405	1 / f_{ADC}

A typical ADC application is shown below:

Figure 7-10 Typical application of ADC



The following formula is used to calculate the maximum value of the external input impedance so that the sampling error can be less than 0.5 LSB:

$$R_{AIN} = M/(f_{ADCCLK} * C_{ADC} * (N+1) * \ln 2) - R_{ADC}$$

Where f_{ADCCLK} is the ADC operating clock frequency, configured by the ADC_CR.CLK bit field; M is the number of sampling clocks, configured by the ADC_SAMPLE.SQRCHy bit field; N is the ADC resolution, and N=12.

The following table shows the relationship between the ADC operating clock frequency f_{ADCCLK}, the number of sampling clocks, and the external input impedance R_{AIN} for a sampling error of 0.5LSB:

Table 7-28 Maximum input impedance table

Number of sampling clocks	R_{AIN} MAX		
	f_{ADCCLK} = 48MHz	f_{ADCCLK} = 24MHz	f_{ADCCLK} = 4MHz
6	1.7kΩ	5kΩ	40kΩ
7	2.3kΩ	6kΩ	46kΩ
9	3.4kΩ	8kΩ	60kΩ
12	5kΩ	12kΩ	81kΩ
18	8kΩ	19kΩ	123kΩ
30	15kΩ	33kΩ	206kΩ
70	38kΩ	79kΩ	484kΩ
134	75kΩ	153kΩ	928kΩ
198	113kΩ	227kΩ	1370kΩ
390	224kΩ	449kΩ	2700kΩ

Table 7-29 Accuracy of ADC[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max. [2]	Unit
ET	Composite error	f_{ADC} = 48MHz, V_{DD} = 1.62V ~ 5.5V, T_A = -40°C ~+85°C	-	±2.5	±3.0	LSB
EO	Offset error		-	±1.5	±2.4	
EG	Gain error		-	±2.2	±2.7	
DNL	Differential nonlinearity		-	±0.5	±1.0	
INL	Integral nonlinearity		-	±1.0	±4.0	
SINAD	Signal-to-noise ratio distortion		-	67	-	dB
SNR	Signal-to-noise ratio		-	66	-	
THD	Total harmonic distortion		-	-70	-	
ENOB	Significant digits	V_{DD} = 1.8V	-	9.8	-	bits
		V_{DD} = 2.8V	-	10.1	-	
		V_{DD} = 3.3V	-	10.3	-	
		V_{DD} = 5.5V	-	10.5	-	

Caution 1 : ADC DC accuracy values are measured after internal calibration;

Avoid injecting reverse current on any analogue input pin as this can degrade the accuracy of conversions performed on another analogue input, it is recommended to add a Schottky diode (between the pin and ground) to the analogue pin where the reverse current will probably be injected;

Better performance can be achieved over restricted V_{DD}, frequency, and temperature ranges.

Caution 2 : Data based on characterization results, not tested in production.

7.3.14 Temperature sensor characteristics

Table 7-30 TS characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L	V_{SENSE} linearity with temperature	-	±2	±5	°C
Avg_Slope	Average slope	2.52	2.55	2.58	mV / °C
V_{25}	Voltage at 25°C (±5°C)	0.75	0.77	0.79	V
t_{START}	TS internal temperature sensor settling time	-	-	40	μs

7.3.15 Analog voltage comparator characteristics

Table 7-31 Comparator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max. [1]	Unit
V_{DD}	Supply volgate	-	1.62	-	5.5	V
V_{IN}	Input volgate range	-	0	-	V_{DD}	V
t_{START}	Startup time	Low speed	-	0.5	-	μs
		High speed	-	0.5	-	
t_D	Delay time	Low speed	-	3	7	
		High speed	-	0.1	0.2	
V_{offset}	Offset error	-	-	±3	±10	mV
$I_{DD(VC)}$	Current consumption	Low speed[2]	-	0.25	0.39	μA
		High speed[3]	-	39	55	
V_{hys}	Comparator hysteresis	VCx_CR0.HYS=0	-	0	-	mV
		VCx_CR0.HYS=1	-	20	-	

Caution 1: Data based on characterization results, not production tested.

Caution 2: This power dissipation increases by 21μA~29μA when the negative source is selected with a built-in 1.2V reference.

Caution 3: This power consumption consists of two parts: the VC's own power consumption and the BGR module power consumption.

7.3.16 Programmable low voltage detector characteristics

Table 7-32 Programmable low voltage detector characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	-	0	-	V_{DD}	V
V_{TH}	Detection threshold	LVD_CR0.VTH = 0	0.95 V_{TH}	1.8	1.05 V_{TH}	
		LVD_CR0.VTH = 1		2.2		
		LVD_CR0.VTH = 2		2.6		
		LVD_CR0.VTH = 3		3.0		
		LVD_CR0.VTH = 4		3.4		
		LVD_CR0.VTH = 5		3.8		
		LVD_CR0.VTH = 6		4.2		
		LVD_CR0.VTH = 7		4.6		
I_{DD}	Power consumption	-	-	760	-	nA
t_{resp}	Response time	-	-	10	-	μs
t_{setup}	Set-up time	-	-	10	-	μs
V_{hys}	Hysteresis voltage	-	-	40	-	mV

7.3.17 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to section *7.3.11 I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 7-33 Timer characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{res(TIM)}$	Timer resolution	-	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 48MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency	-	-	-	f_{TIMCLK} / 2	MHz
t_{MAX_COUNT}	Maximum period	-	-	-	65536	t_{TIMCLK}

7.3.18 Communication interfaces

I2C interface characteristics

- The I2C interface meets the I2C-bus specification and the user manual:
  - Standard-mode (Sm): with a bit rate up to 100 kbit/s
  - Fast-mode (Fm) : with a bit rate up to 400 kbit/s
  - Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s
- The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).
- The SDA and SCL I/O requirements are met with the following restrictions:
  - The SDA and SCL I/O pins are not "true" open-drain,maximum input voltage limited by specification.

    When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present.

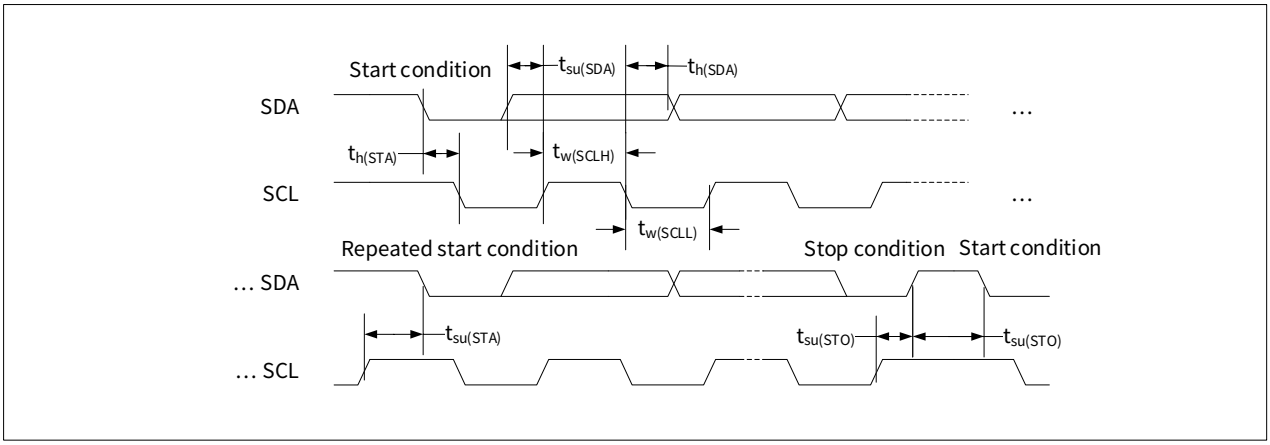
Refer to Section *7.3.11 I/O port characteristics* for the I2C I/Os characteristics.

Table 7-34 I2C characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.25	-	0.5	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	50	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{h(STA)}$	Start condition hold time	2.5	-	0.625	-	0.25	-	µs
$t_{su(STA)}$	Repeated Start Condition Startup Time	2.5	-	0.6	-	0.25	-	
$t_{su(STO)}$	Stop condition setup time	0.25	-	0.25	-	0.25	-	
$t_{w(STO:STA)}$	Stop condition to start condition time(Bus Idle)	4.7	-	1.3	-	0.5	-	

Caution 1: Guaranteed by design, not tested in production.

Figure 7-11 I2C timing diagram



SPI interface characteristic parameters

Table 7-35 SPI characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{SCK}	SPI clock frequency	Master mode PCLK = 48MHz	41.6	-	ns
		Slave mode	28.5	-	
$t_{su(NSS)}$	NSS setup time	Slave mode	1 * t_{PCLK}	-	
$t_{h(NSS)}$	NSS hold time	Slave mode	1.0	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low setup time	Master mode/Slave mode	0.5 * $t_{c(SCK)}$	-	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	1.0	-	
		Slave mode	1.0	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	1.0	-	
		Slave mode	2.0	-	
$t_{v(SO)}$	Data output valid time	Slave mode	-	10.0	
$t_{h(MO)}$	Data output hold time	Master mode	2.1	-	

Caution 1: Data based on characterization results, not tested in production.

Figure 7-12 SPI timing diagram - slave mode and CPHA=0

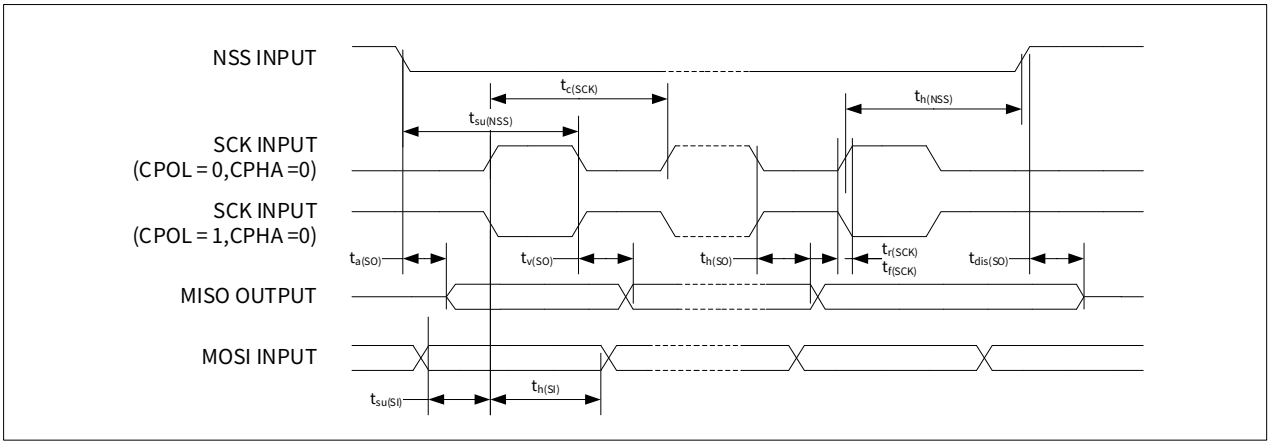


Figure 7-13 SPI timing diagram - slave mode and CPHA=1

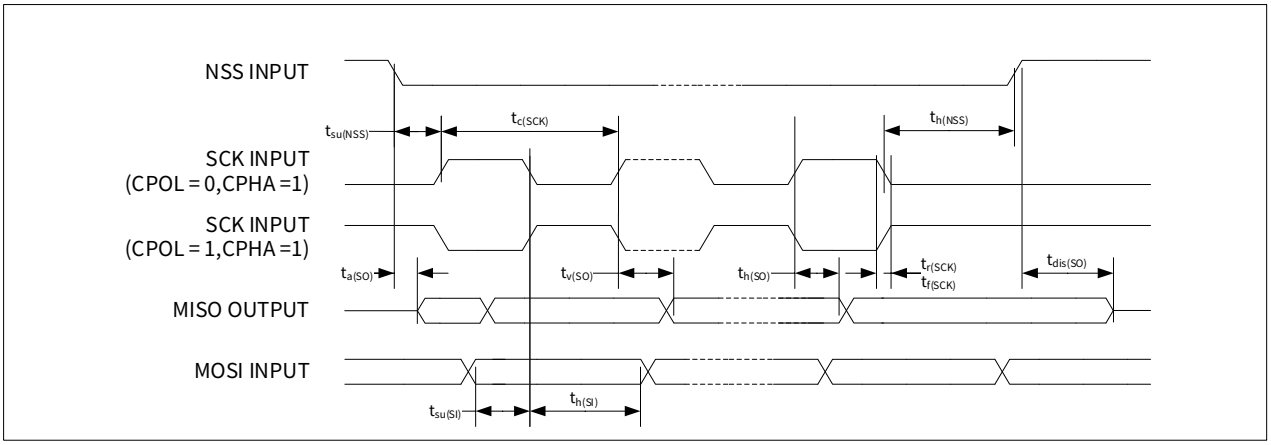
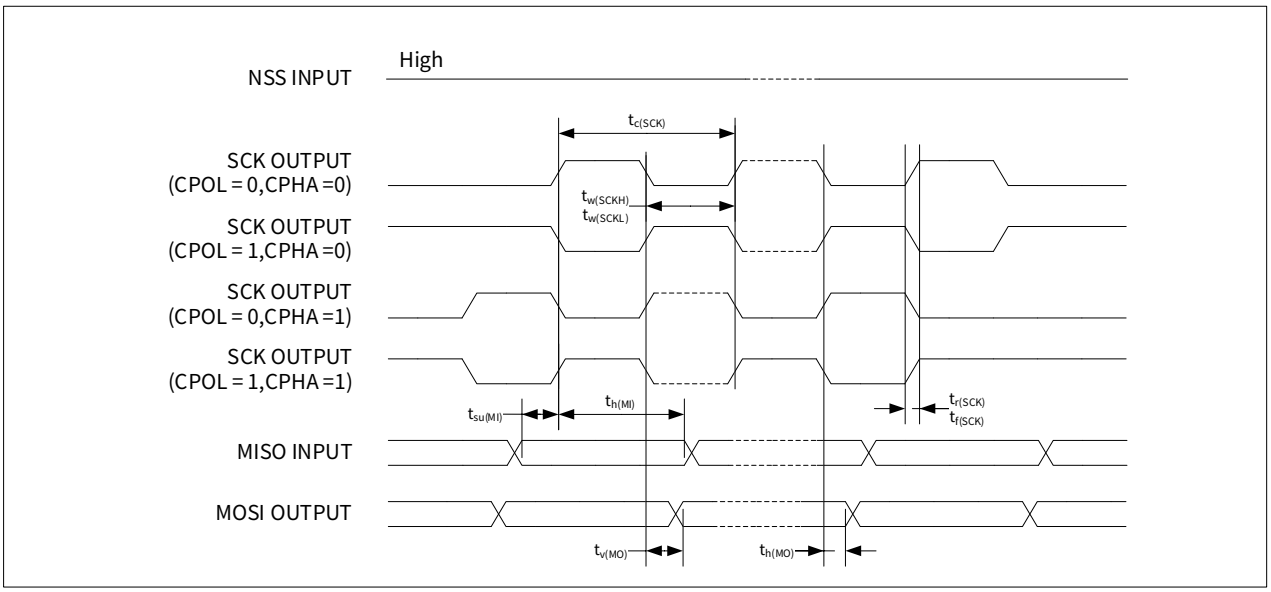


Figure 7-14 SPI timing diagram - master mode

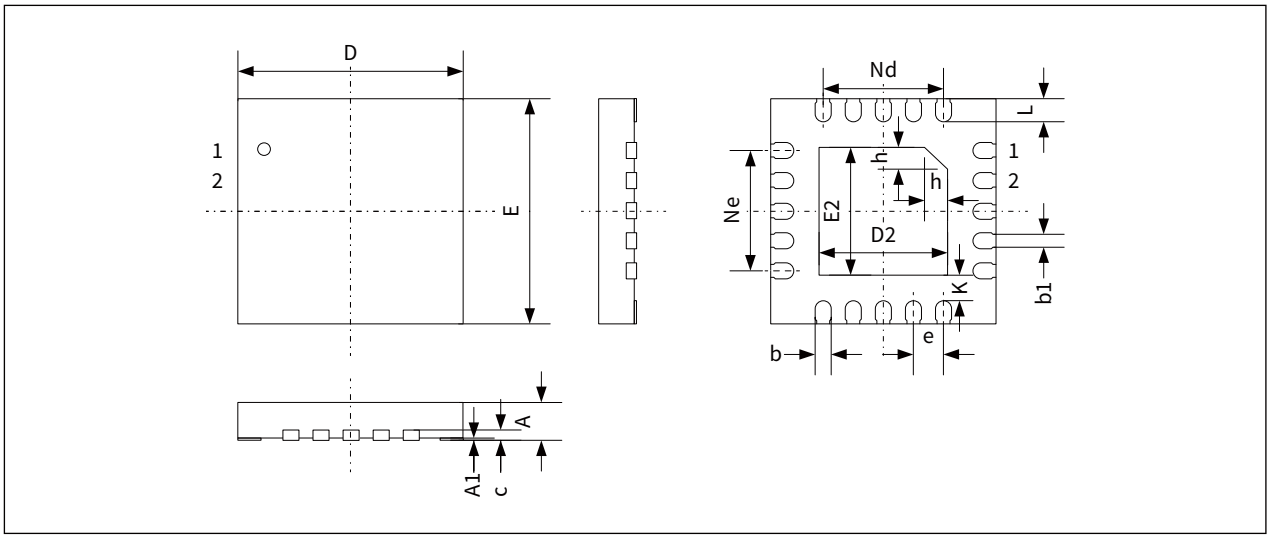


8 Package information

8.1 QFN20 package information

QFN20 is 20-pin, 3.0 * 3.0mm Quad flat no-leads package.

Figure 8-1 QFN20 outline



Caution 1: Drawing is not to scale.

Table 8-1 QFN20 mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.020	0.050	-	0.0008	0.0020
b	0.150	0.200	0.250	0.0059	0.0079	0.0098
b1	0.140REF			0.0055REF		
c	0.150REF			0.0059REF		
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
D2	1.600	1.700	1.800	0.0630	0.0669	0.0709
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
E2	1.600	1.700	1.800	0.0630	0.0669	0.0709
e	0.400 BSC			0.0157 BSC		
K	0.250	0.350	0.450	0.0098	0.0138	0.0177
L	0.300	0.350	0.400	0.0118	0.0138	0.0157
h	0.250	0.300	0.350	0.0098	0.0118	0.0138
Ne	1.600 BSC			0.0630 BSC		
Nd	1.600 BSC			0.0630 BSC		

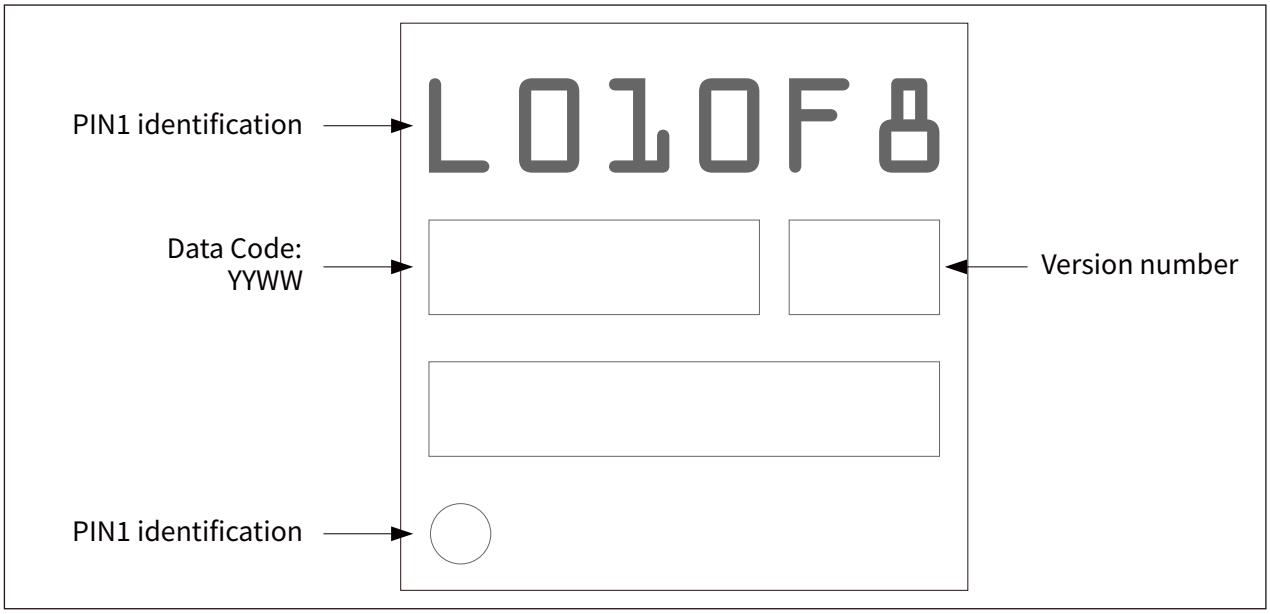
Caution 1: Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-2 QFN20 topside marking example

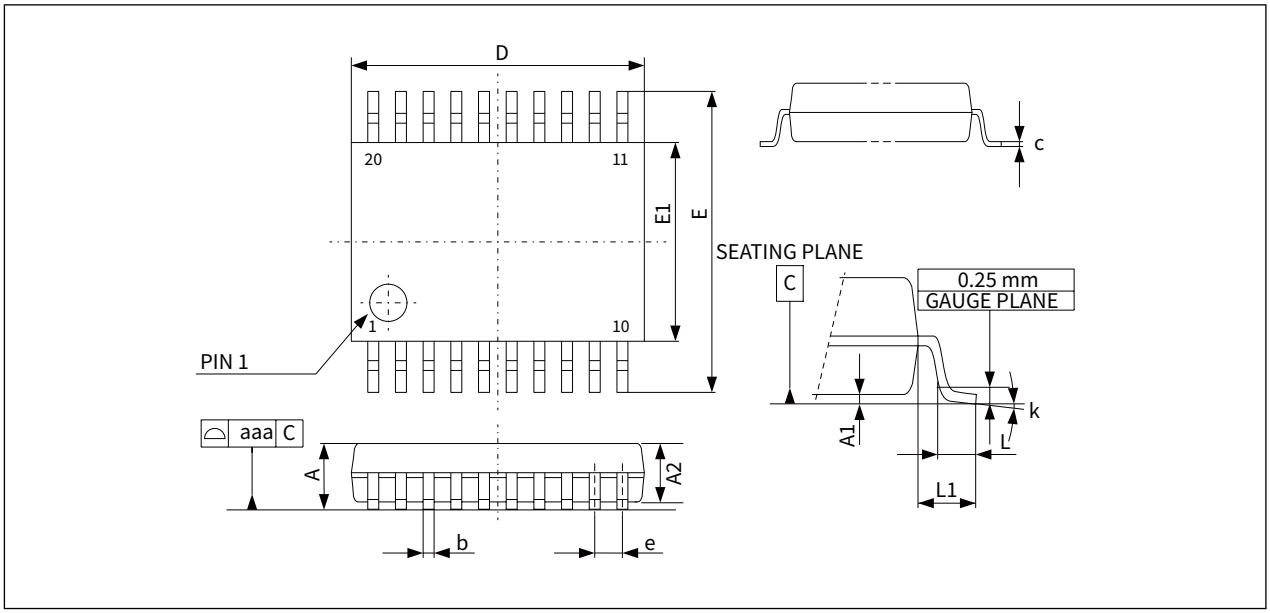


Caution 1: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.2 TSSOP20 package information

TSSOP20 is a 20-pin, 6.5 * 4.4mm Thin shrink small outline 0.65mm pitch package.

Figure 8-3 TSSOP20 outline



Caution 1: Drawing is not to scale.

Table 8-2 TSSOP20 mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

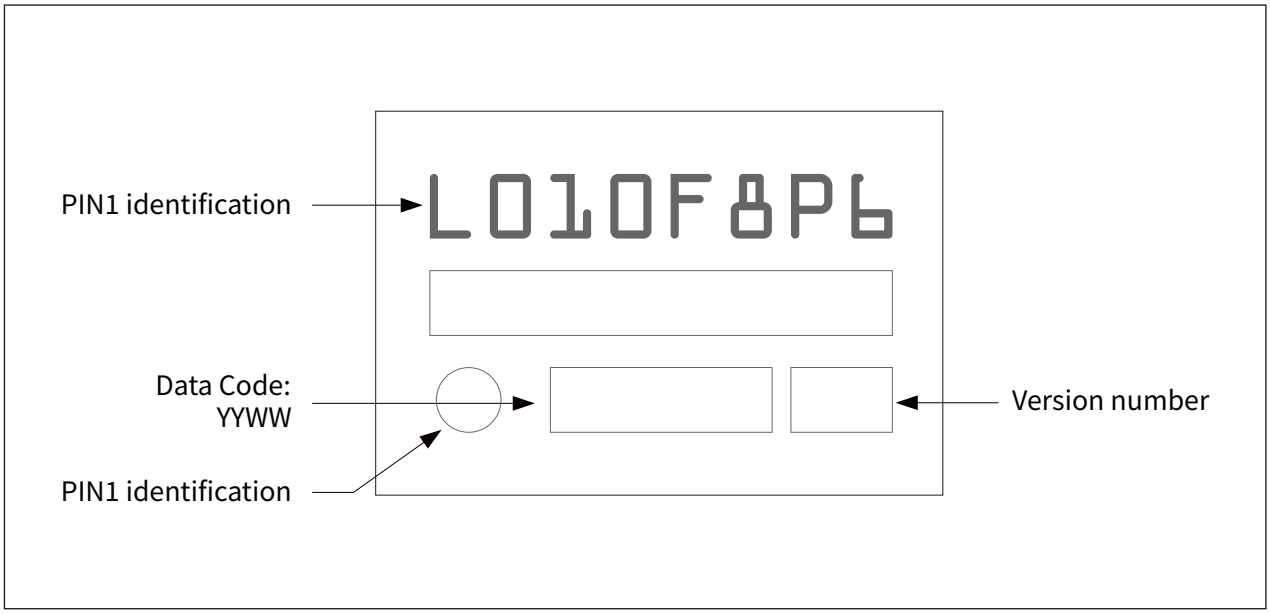
Caution 1: Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-4 TSSOP20 topside marking example

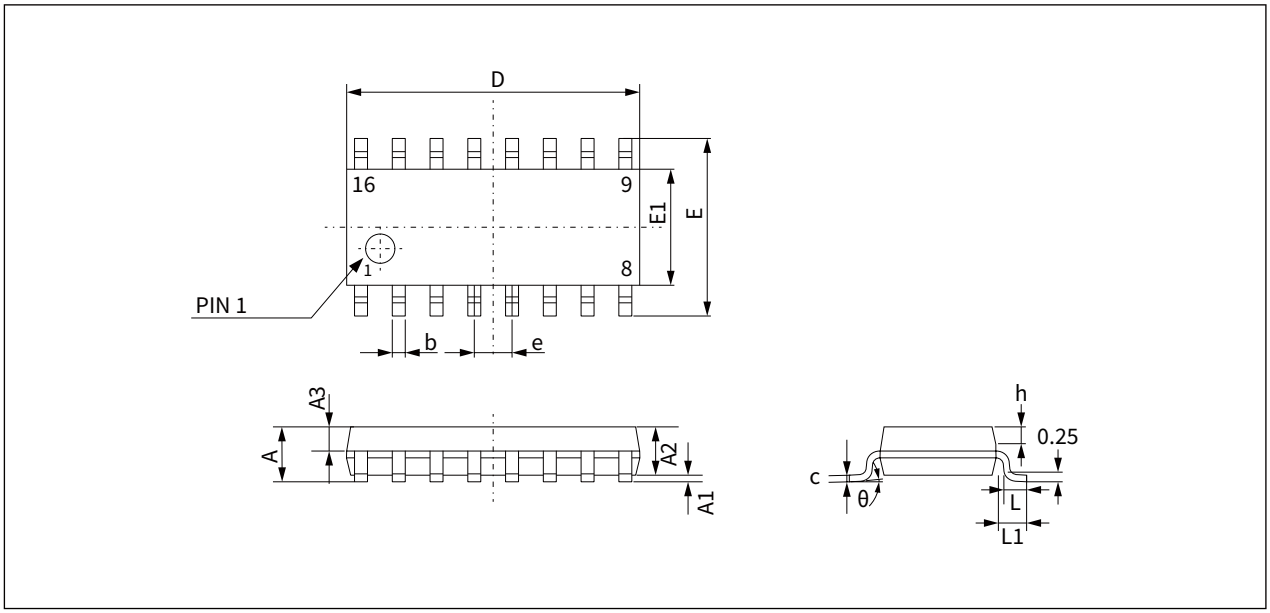


Caution 1: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.3 SOP16 package information

SOP16 is a 16-pin, 9.9 * 3.9mm Small outline 1.27mm pitch package.

Figure 8-5 SOP16 outline



Caution 1: Drawing is not to scale.

Table 8-3 SOP16 mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.75	-	-	0.0689
A1	0.10	-	0.225	0.0039	-	0.0089
A2	1.30	1.40	1.50	0.0512	0.0551	0.0591
A3	0.60	0.65	0.70	0.0236	0.0256	0.0276
b	0.39	-	0.47	0.0154	-	0.0185
c	0.20	-	0.24	0.0079	-	0.0094
D	9.80	9.90	10.00	0.3858	0.3898	0.3937
E	5.80	6.00	6.20	0.2283	0.2362	0.2441
E1	3.80	3.90	4.00	0.1496	0.1535	0.1575
e	1.27BSC			0.0500BSC		
h	0.25	-	0.50	0.0098	-	0.0197
L	0.50	-	0.80	0.0197	-	0.0315
L1	1.05REF			0.0413REF		
θ	0	-	8°	0	-	8°

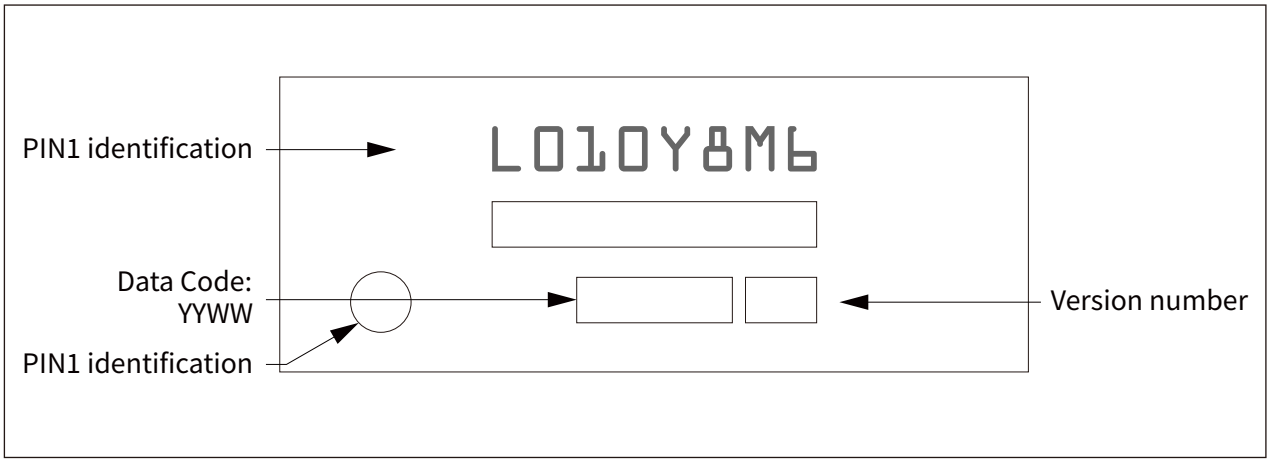
Caution 1: Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-6 TSSOP20 topside marking example



Caution 1: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.4 Thermal characteristics

The maximum chip junction temperature $T_J$max must never exceed the values given in *Table 7-3 Thermal characteristics*.

The maximum chip-junction temperature, $T_J$max, in degrees Celsius, may be calculated using the following equation:

$$T_J\text{max} = T_A\text{max} + (P_D\text{max} \times \Theta_{JA})$$

Where:

- $T_A$max is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C /W
- $P_D$max is the sum of P_{INT}max and $P_{I/O}$max ($P_D$max = P_{INT}max + $P_{I/O}$max)
- P_{INT}max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power
- $P_{I/O}$max represents the maximum power dissipation on output pins, where:

$$P_{I/O}\text{max} = \Sigma\ (V_{OL} \times I_{OL}) + \Sigma\ ((V_{DD} - V_{OH}) \times I_{OH})$$

The actual level and current conditions of the I/Os need to be included in the accurate calculation.

Table 8-4 Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient QFN20 – 3.0mm * 3.0mm	90	°C /W
	Thermal resistance junction-ambient TSSOP20 – 6.5mm * 4.4mm	76	
	Thermal resistance junction-ambient SOP16 – 9.9mm * 6.0mm	95	

8.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from *www.jedec.org*

9 Ordering information

Example: CW32L010F8U6x

Device family
CW32=ARM-based

Product type
L=Lower power

Sub-family
010=CW32L010xx

Pin count
F=20 pins
K=32 pins
C=48 pins
Y=16 pins

Code size
6=32Kbytes Flash
8=64Kbytes Flash

Package
M=SOP
P=TSSOP
T=LQFP
U/V=QFN

Temperature range
6=-40°C~85°C
7=-40°C~105°C

Option
xxx=Programmed part
TR=Tape and reel

Table 9-1 Minimum Order Quantity (MOQ)

MCU	Packaging	Quantity	MOQ	MSL	Note
CW32L010F8U6	Reel	5000 pcs/reel	5000 pcs	3	1 reels/box, 8 boxes/carton, single reel vacuumized
CW32L010F8P6	Tube	70 pcs/tube	7000 pcs	3	50 tubes/bundle, 2 bundles/box, 10 boxes/carton, single box vacuumized
CW32L010Y8M6	Tube	500 pcs/tube	10000 pcs	3	200 tubes/box, single box vacuumized

10 Revision history

Table 10-1 Document revision history

Date	Revision	Changes
November 4, 2024	Rev 1.0	Initial release.