



武汉芯源半导体有限公司

WUHAN XINYUAN SEMICONDUCTOR CO., LTD

CW32A030 Datasheet

ARM® Cortex®-M0+ 32-bit MCU with up to 64KB FLASH, 8KB RAM

Rev 1.0

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1 Features

- Core: ARM® Cortex®-M0+
 - Frequency up to 64MHz
- Operating temperature: -40°C to 105°C ; Operating voltage: 1.65V to 5.5V
- Memories
 - Maximum 64 Kbytes FLASH, data retention 25 years @85°C
 - Up to 8 Kbytes RAM, support parity
 - 128 bytes OTP memory
- CRC calculation unit
- Reset and power management
 - Low power modes (Sleep, DeepSleep)
 - Power-on/Power down reset (POR/BOR)
 - Programmable low voltage detector (LVD)
- Clock management
 - 4 to 32 MHz crystal oscillator
 - 32kHz low speed crystal oscillator
 - Internal 48 MHz RC oscillator
 - Internal 32 kHz RC oscillator
 - Internal 10 kHz RC oscillator
 - Internal 150 kHz RC oscillator
 - Internal PLL phase-locked loop
 - Clock monitoring system
 - Allow independent shutdown of each peripheral clock
- Up to 39 I/O ports
 - All I/Os support interrupt function
 - All I/Os support interrupt input filtering
- 5-channel DMA controller
- Analog to digital converter
 - 12-bit accuracy, ± 1 LSB
 - Up to 1M SPS conversion speed
 - Internal voltage reference
 - Analog watchdog function
 - Internal temperature sensor
- Dual voltage comparator

- Real Time Clock and Calendar
 - Support wakeup from Sleep/DeepSleep mode
- Timers
 - One 16-bit advanced-control timer for six-channel capture/compare and 3 pairs of complementary PWM output,dead time and flexible synchronization function
 - Four groups of 16-bit general-purpose timers
 - Three groups of 16-bit basic timers
 - Window watchdog timer
 - Independent watchdog timer
- Communication interfaces
 - Three-way low-power UART with fractional baud rate
 - Two SPIs (12Mbit/s)
 - Two I2Cs (1Mbit/s)
 - IR modulator
- Serial wire debug (SWD)
- 80-bit unique ID
- AEC-Q100 (Grade 2) Vehicle Standard

Table 1-1 Package model list

| Series | Model | Packages |
|------------|------------|----------|
| CW32A030x8 | CW32A030C8 | LQFP48 |

2 Introduction

This datasheet provides the ordering information and electromechanical characteristics of the CW32A030 microcontrollers.

This document should be read in conjunction with the CW32A030 reference manual.

For information on the Arm® Cortex®-M0+ core, please refer to the Cortex®-M0+ Technical Reference Manual, available from the www.arm.com.

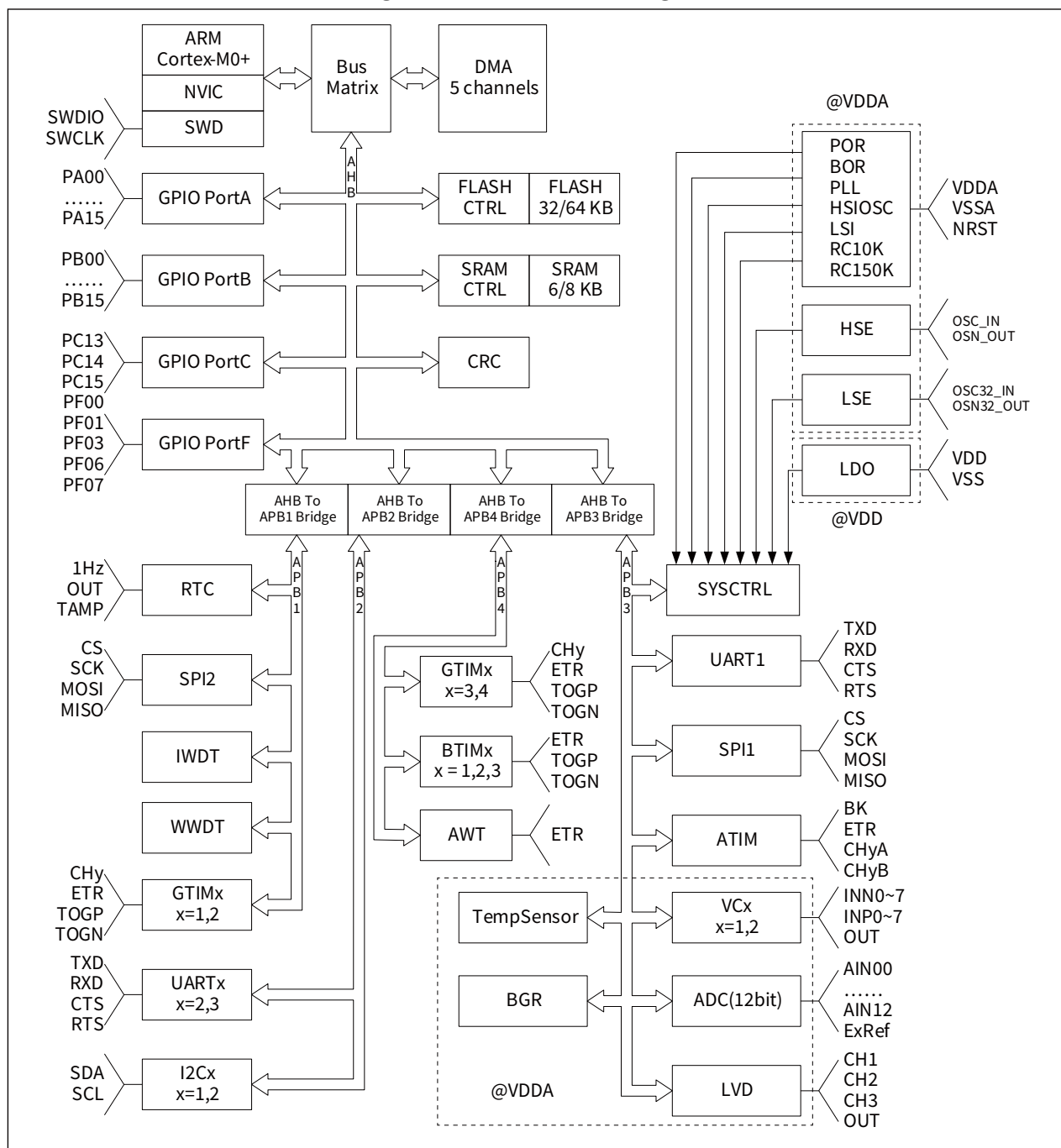
3 Description

CW32A030 is an eFlash-based single-chip microcontroller that integrates an ARM® Cortex®-M0+ core with a main frequency up to 64MHz, high-speed embedded memories(up to 64 Kbytes of FLASH and up to 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os.

All devices offer standard communication interfaces (three UARTs, two SPIs, two I2Cs), one 12-bit ADC, seven general-purpose and basic timers and an advanced-control PWM timers.

CW32A030 operates in the -40°C to 105°C temperature range from a 1.65 to 5.5V power supply, supports two low-power operating modes (Sleep and DeepSleep). The internal block diagram is shown in the following figure:

Figure 3-1 Internal block diagram



CW32A030 provides LQFP48 package. The details are shown in the following table:

Table 3-1 CW32A030 family device features list

| Peripheral | | CW32A030C8T7 |
|------------------------------------|------------------|-------------------------|
| FLASH (Kbytes) | | 64 |
| SRAM (Kbytes) | | 8 |
| Timers | Advanced control | 1 |
| | General purpose | 4 |
| | Basic | 3 |
| SPI | | 2 |
| I2C | | 2 |
| UART | | 3 |
| 12-bit ADC (number of channels) | | 1 (13 ext. + 3 int.) |
| GPIO | | 39 |
| Kernel frequency | | 64MHz |
| Operating voltage | | 1.65V ~ 5.5V |
| Operating temperature | | -40°C ~ 105°C |
| Packages | | LQFP48 |

4 Functional overview

4.1 ARM® Cortex®-M0+ core with embedded Flash and SRAM

The Arm® Cortex®-M0+ processor is the latest generation 32-bit core for small embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The Arm® Cortex®-M0+ 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the small memory.

The CW32A030 family has an embedded Arm core and is therefore compatible with all Arm tools and software.

4.2 Memories

The device has the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for high reliability critical applications.
- The non-volatile memory is divided into two arrays:
 - 64 Kbytes bytes of embedded Flash memory for programs and data
 - 2.5 Kbytes of boot program memory
- FLASH memory erasing and reading protection: The FLASH memory erasing and writing protection is performed through the register, and the 4-level read protection level is set through the ISP command.
 - LEVEL0
No readout protection, the FLASH memory can be read by SWD or ISP.
 - LEVEL1
FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP or SWD interface. After the downgrade, the FLASH is in the whole chip erasing state.
 - LEVEL2
FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP interface. After the downgrade, the FLASH is in the whole chip erasing state.
 - LEVEL3
FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. Protection level downgrade in any way is not supported.

4.3 Boot mode

At startup, the BOOT pin can be used to select the following two startup options:

- Run the internal bootloader
- Run user program

When running the Bootloader, the user can use the ISP communication protocol for FLASH programming through UART1 (pins are PA13/PA14).

4.4 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit can generate the CRC code of the data stream according to the selected algorithm and parameter configuration.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

The product supports ten commonly used CRC algorithms, including:

- CRC16_IBM
- CRC16_MAXIM
- CRC16_USB
- CRC16_MODBUS
- CRC16_CCITT
- CRC16_CCITT_FALSE
- CRC16_X25
- CRC16_XMODEM
- CRC32
- CRC32_MPEG2

4.5 Power management

4.5.1 Power supply schemes

- $V_{DD} = 1.65V$ to $5.5V$
External power supply for I/Os and the internal regulator. Provided externally through VDD pins.
- $V_{DDA} = 1.65V$ to $5.5V$
External analog power supply for ADC, Reset blocks, RCs and PLL. Accessed through VDDA pin. The V_{DDA} voltage must be always greater or equal to the V_{DD} voltage.

For details about the power supply, refer to [Figure 7-3 Power system](#).

4.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (BOR) circuits. They are always active, the device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/BOR}$, without the need for an external reset circuit.

The POR/BOR monitors both the VDD and VDDA supply voltages. In order to ensure that the chip works normally after the reset is released, it is necessary to ensure that VDD/VDDA is powered on and off at the same time in the circuit design.

4.5.3 Voltage regulator

The internal voltage regulator has "normal" and "low power" operating modes, and it always enabled after reset.

- The "normal" mode corresponds to a state of full speed operation.
- The "low-power" mode corresponds to some power supply working states, including Sleep and DeepSleep working modes.

4.5.4 Low-power modes

The CW32A030 microcontrollers support two low-power modes:

- Sleep mode
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- DeepSleep mode
DeepSleep is used to achieve the lowest power consumption, the CPU stops running, the high-speed clock modules (HSE, HSIOSC) are automatically turned off, and the low-speed clocks (LSE, LSI, RC10K, RC150K) remain unchanged.
The device exits DeepSleep mode when an external reset, or an IWDT reset, or some peripheral interrupts, or an RTC event occurs.

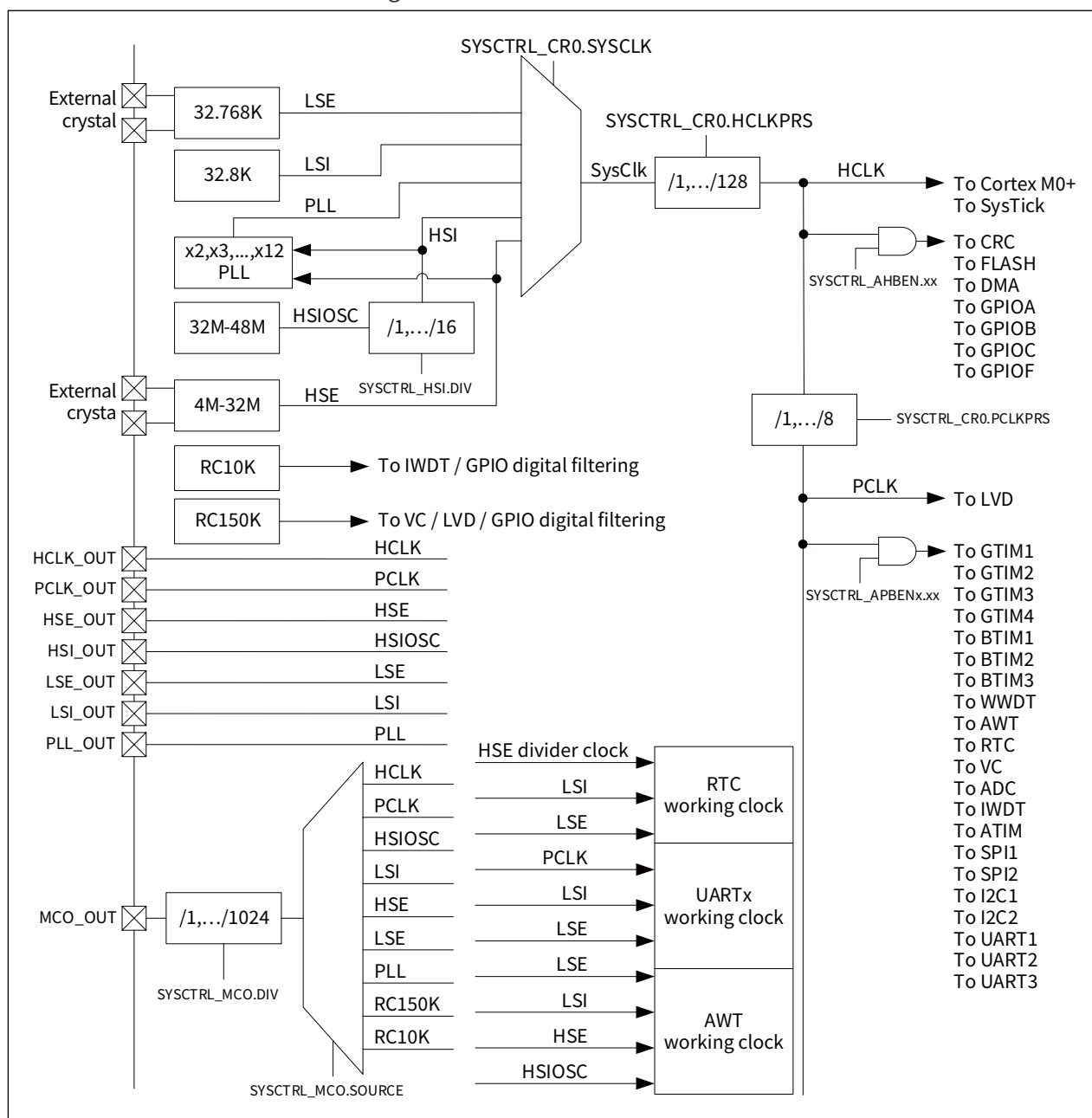
4.6 Clocks and startup

After the MCU is reset, the HSI (generated by the internal 48MHz HSIOSC oscillator frequency division) is selected as the clock source of SysClk by default, and the default value of the system clock frequency is 8MHz. The user can use the program to start the external crystal oscillator and switch the system clock source to the external clock source. The clock failure detection module can continuously detect the state of the external clock source. Once the failure of the external clock source is detected, the system will automatically switch to the internal HSIOSC clock source. If the corresponding fault detection interrupt is enabled, an interrupt will be generated for the user to record fault events.

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 64 MHz.

The internal clock tree of the system is shown below :

Figure 4-1 Clock tree of CW32A030



4.7 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Some GPIO pins have analog functions and interface with internal analog peripherals. All I/Os can be configured as external interrupt input pins and have digital filtering.

The response speed and drive capability of GPIO can be selected from two gears. For details, please refer to the data and charts in the relevant chapters.

The I/O configuration can be locked to prevent program misoperation and improve security. GPIO supports separate access operations of high and low bytes to speed up user program operation.

4.8 Direct memory access controller (DMA)

The chip has a built-in DMA controller, 5 independent channels, high-speed data transmission between peripherals and memory, between peripherals and peripherals, and between memory and memory.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. The software can configure the transmission direction and data length of each channel individually.

4.9 Nested vectored interrupt controller (NVIC)

The CW32A030 family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0+) and supports programmable 4 priority levels.

- Interrupt entry vector table address can be remapped
- Closely coupled NVIC core interface
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved

This hardware block provides flexible interrupt management features with minimal interrupt latency.

4.10 Analog to digital converter (ADC)

The internal 12-bit analog to digital converter has up to 13 external and three internal (temperature sensor, voltage reference measurement, VDDA/3) channels and performs conversions in single-shot or scan modes.

In scan mode, automatic conversion is performed on a selected group of analog inputs.

High-precision voltage reference can be externally connected.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of a selected channel. An interrupt is generated when the converted voltage is outside the programmed thresholds.

4.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN14 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of temperature sensor measurement, manufacturers perform individual factory calibrations for each chip. Temperature sensor factory calibration data is stored in FLASH memory.

Table 4-1 Internal temperature sensor calibration value address

| ADC reference voltage | Calibration value storage address | Calibration value accuracy |
|-----------------------|-----------------------------------|----------------------------|
| Internal 1.5V | 0x0001 260A - 0x0001 260B | $\pm 3^{\circ}\text{C}$ |
| Internal 2.5V | 0x0001 260C - 0x0001 260D | $\pm 3^{\circ}\text{C}$ |

4.10.2 Internal voltage reference

In addition to VDDA and external reference voltage, ADC reference voltage can also choose internal reference voltage. The internal reference voltage generator (BGR) can provide stable voltage output for ADC, which is 1.5V and 2.5V respectively.

4.11 Timers and watchdogs

The CW32A030 microcontroller integrates up to four general-purpose timers, three basic timers and one advanced control timer.

The function differences of different timers are shown in the following table:

Table 4-2 Timer feature comparison

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|------------------|-------|--------------------|-------------------|------------------|------------------------|--------------------------|-----------------------|
| Advanced control | ATIM | 16-bit | Up, down, up/down | $2^N(N=0,..7)$ | YES | 6 | 3 |
| General purpose | GTIM1 | 16-bit | Up, down, up/down | $2^N(N=0,..15)$ | YES | 4 | 1 |
| | GTIM2 | 16-bit | Up, down, up/down | $2^N(N=0,..15)$ | YES | 4 | 1 |
| | GTIM3 | 16-bit | Up, down, up/down | $2^N(N=0,..15)$ | YES | 4 | 1 |
| | GTIM4 | 16-bit | Up, down, up/down | $2^N(N=0,..15)$ | YES | 4 | 1 |
| Basic | BTIM1 | 16-bit | Up | $2^N(N=0,..15)$ | YES | 0 | 1 |
| | BTIM2 | 16-bit | Up | $2^N(N=0,..15)$ | YES | 0 | 1 |
| | BTIM3 | 16-bit | Up | $2^N(N=0,..15)$ | YES | 0 | 1 |

4.11.1 Advanced-control timer (ATIM)

The Advanced-control Timer (ATIM) consists of a 16-bit auto-reload counter and 7 compare units, driven by a programmable prescaler. ATIM supports 6 independent capture/compare channels, which can realize 6 independent PWM outputs or 3 pairs of complementary PWM outputs or capture 6 inputs. Can be used for basic timing/counting, measuring pulse width and period of input signals, generating output waveforms (PWM, single pulse, complementary PWM with dead time inserted, etc.).

4.11.2 General-purpose timers (GTIM1..4)

Four general-purpose timers (GTIMs) are integrated inside. Each GTIM is completely independent and has the same function. Each includes a 16-bit automatic reloading counter and is driven by a programmable prescaler. GTIM supports 4 basic working modes: timer mode, counter mode, trigger start mode and gate control mode. Each group has 4 independent capture/compare channels, which can measure the pulse width of input signals (input capture) or generate output waveforms (output compare and PWM).

4.11.3 Basic timers (BTIM1..3)

Three basic timers (BTIM) are integrated inside, each BTIM is completely independent and has the same function, each contains a 16-bit automatic reloading counter and is driven by a programmable prescaler. BTIM supports four working modes: timer mode, counter mode, trigger start mode and gate control mode, and supports overflow event trigger interrupt request and DMA request. Thanks to the fine processing design of the trigger signal, the BTIM can automatically perform the filtering operation of the trigger signal by the hardware, and can also cause the trigger event to generate interrupts and DMA requests.

4.11.4 Independent watchdog (IWDT)

The Independent Watchdog Timer (IWDT) uses a dedicated internal RC clock source, RC10K, to avoid external influences during operation. Once the IWDT is started, the user needs to reload the counter of the IWDT within a specified time interval, otherwise an overflow will trigger a reset or generate an interrupt signal. After the IWDT is started, the counting can be stopped. The user can choose to keep the IWDT running or suspend counting while in DeepSleep mode.

A specially set key-value register can lock the key registers of the IWDT to prevent the registers from being accidentally modified.

4.11.5 System window watchdog (WWDT)

The CW32A030 microcontroller integrates a window watchdog timer (WWDT), the user needs to refresh within the set time window, otherwise the watchdog overflow will trigger a system reset. WWDT is usually used to monitor the program execution flow with strict time requirements to prevent the abnormal execution of the application program caused by external interference or unknown conditions, resulting in system failure.

4.11.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0

4.12 Real-time clock (RTC)

The Real Time Clock (RTC) is a dedicated counter/timer that provides calendar information including hours, minutes, seconds, date, month, year, and week day.

RTC has two independent alarm clocks, the time and date can be set in combination, and the alarm clock interrupt can be generated and output through the pin; it supports the time stamp function, which can be triggered by the pin, record the current date and time, and generate a time stamp interrupt at the same time; Support periodic interrupt; support automatic wake-up function, which can generate interrupts and output through pins; support 1Hz square wave and RTCOUT output functions; support internal clock calibration compensation.

The CW32A030 has internal independently calibrated RC clock source with a frequency of 32kHz to provide the drive clock for the RTC. The RTC can run in DeepSleep mode and is suitable for applications requiring low power consumption.

4.13 Inter-integrated circuit interfaces (I2C)

The I2C controller can serially send the data to be sent to the I2C bus according to the I2C specification according to the set transmission rate (standard, fast, high-speed), and detect the state during the communication process. I2C also support bus conflict and arbitration handling in multi-master communication.

The main features of the I2C controller are:

- Supports master send/receive and slave send/receive four working modes
- Supports clock stretching (clock synchronization) and multi-master communication collision arbitration
- Supports standard (100Kbps)/fast (400Kbps)/high speed (1Mbps) three working rates
- Supports 7-bit addressing mode
- Supports 3 slave addresses
- Supports broadcast address
- Supports input signal noise filtering function
- Supports interrupt status query function

4.14 Universal asynchronous receiver/transmitter (UART)

Universal asynchronous receiver/transmitter (UART) supports asynchronous full-duplex, synchronous half-duplex and single-wire half-duplex modes, supports hardware data flow control and multi-machine communication; the data frame structure is programmable, and a wide range of baud rate selection can be provided through the fractional baud rate generator.

The UART controller works in a dual clock domain, allowing data reception in DeepSleep mode, and the reception completion interrupt can wake the MCU back to Active mode.

4.15 Serial peripheral interface (SPI)

Serial Peripheral Interface (SPI) supports bidirectional full-duplex, single-wire half-duplex and simplex communication modes, MCU can be configured as master or slave, multi-master communication mode is supported, and direct memory access (DMA) is supported.

The main features of the Serial Peripheral Interface (SPI) are:

- Supports master mode, slave mode
- Supports full-duplex, single-wire half-duplex, simplex
- 4-bit to 16-bit selectable data frame width
- Supports sending and receiving data LSB or MSB first
- Clock Polarity and Clock Phase is programmable
- Communication rates up to PCLK/2 in master mode
- Communication rates up to PCLK/4 in slave mode
- Supports multi-machine communication mode
- 8 interrupt sources with flag bits
- Supports Direct Memory Access (DMA)

4.16 Serial wire debug port (SWD)

An ARM SWD interface is provided, and users can use the CW-DAPLINK of Xinyuan Semiconductor to connect to the MCU to debug and simulate in the IDE development environment.

5 Pin descriptions

Figure 5-1 LQFP48 package pinout (top view)

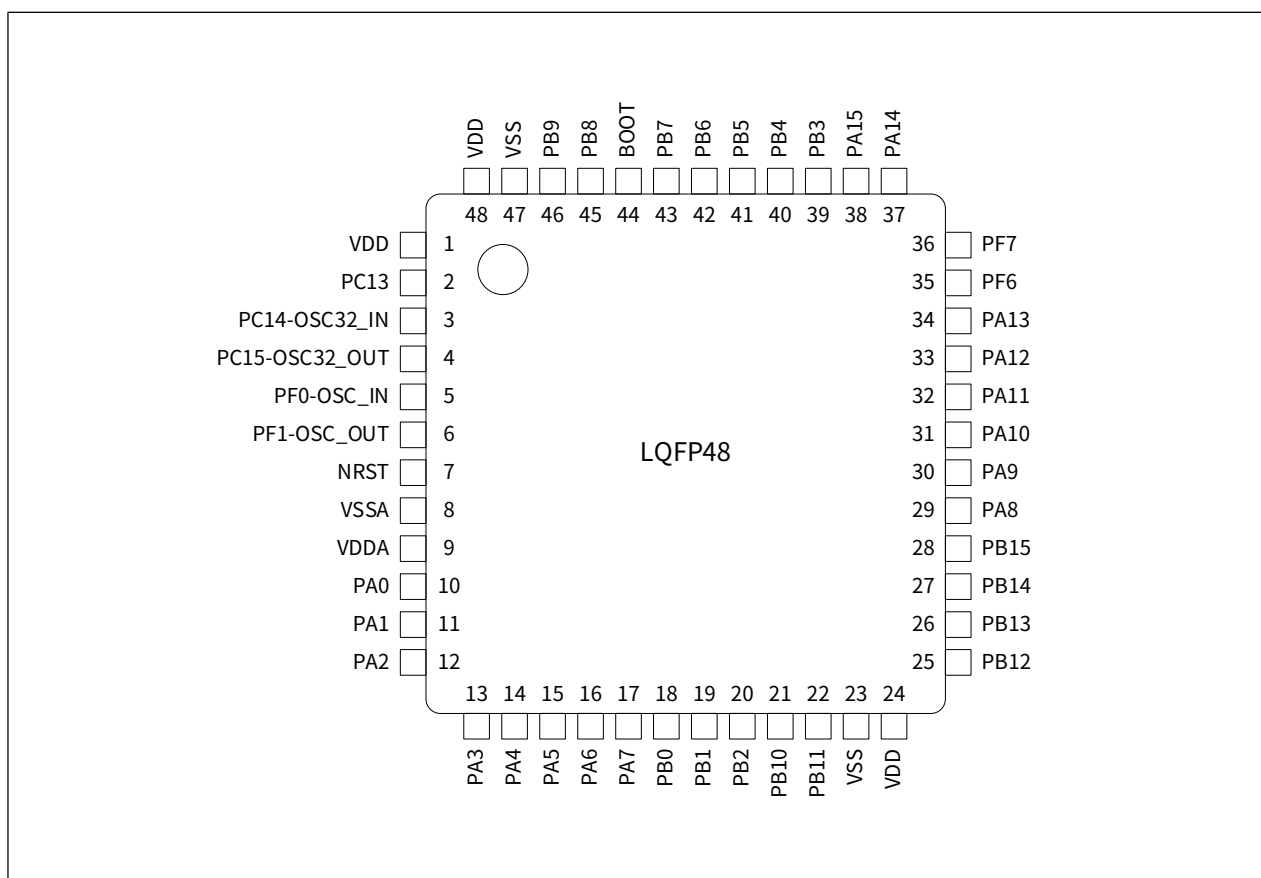


Table 5-1 Legend/abbreviations used in the pinout table

| Name | Abbreviation | Definition |
|----------------------|--|--|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function after reset is the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input / output pin |
| I/O structure | TTa | Connect the I/O port for the analog function |
| | TC | Standard I/O pin |
| | B | Dedicated BOOT pin |
| | RST | Reset input pin |
| Notes | Unless otherwise specified by a note, all pins are set as high impedance input state after reset | |
| Additional functions | Digital function | Functions selected through GPIOx_AFRy registers |
| | Analog function | Functions directly selected through peripheral registers |

Table 5-2 CW32A030 pin definitions

| Pin number | Pin name (function after reset) | Pin type | I/O structure | Notes | Additional functions | |
|------------|------------------------------------|----------|---------------|-------|---|---------------------------|
| LQFP48 | | | | | Digital function | Analog function |
| 1 | VDD | S | - | - | Power supply | |
| 2 | PC13 | I/O | TC | - | PLL_OUT, RTC_1Hz, UART1_CTS, RTC_OUT, BTIM_ETR, GTIM3_ETR, RTC_TAMP | |
| 3 | PC14 | I/O | TC | - | AWT_ETR, GTIM4_CH4, UART1_RTS, BTIM2_TOGP, SPI2_MISO, GTIM3_TOGN, GTIM3_CH1 | OSC32_IN |
| 4 | PC15 | I/O | TC | - | HSE_OUT, GTIM4_CH3, GTIM4_ETR, BTIM2_TOGN, SPI2_MOSI, GTIM3_TOGP, GTIM3_CH2 | OSC32_OUT |
| 5 | PF00 | I/O | TC | - | AWT_ETR, GTIM4_CH2, I2C1_SDA, BTIM1_TOGP, SPI2_SCK, GTIM2_TOGN, GTIM3_CH3 | OSC_IN |
| 6 | PF01 | I/O | TC | - | LSE_OUT, GTIM4_CH1, I2C1_SCL, SPI2_CS, GTIM3_CH4, GTIM2_TOGP, BTIM1_TOGN | OSC_OUT |
| 7 | NRST | I | RST | - | Device reset input | |
| 8 | VSSA | S | - | - | Analog ground | |
| 9 | VDDA | S | - | - | Analog power supply | |
| 10 | PA00 | I/O | TTa | - | UART3_CTS, UART2_CTS, RTC_TAMP, VC1_OUT, SPI2_MISO, GTIM2_CH1, GTIM2_ETR | ADC_IN0, VC1_CH0, LVD_CH1 |
| 11 | PA01 | I/O | TTa | - | UART3_RTS, UART2_RTS, I2C2_SCL, LVD_OUT, SPI2_MOSI, GTIM2_CH2, RTC_TAMP | ADC_IN1, VC1_CH1 |
| 12 | PA02 | I/O | TTa | - | UART3_TXD, UART2_TXD, I2C2_SDA, VC2_OUT, SPI2_SCK, GTIM2_CH3, AWT_ETR | ADC_IN2, VC1_CH2 |
| 13 | PA03 | I/O | TTa | - | UART3_RXD, UART2_RXD, GTIM2_CH2, PCLK_OUT, SPI2_CS, GTIM2_CH4, ATIM_CH3A | ADC_IN3, VC1_CH3 |
| 14 | PA04 | I/O | TTa | - | UART2_CTS, I2C2_SCL, HCLK_OUT, SPI1_CS, GTIM2_ETR, ATIM_CH2A | ADC_IN4, VC1_CH4 |
| 15 | PA05 | I/O | TTa | - | GTIM2_ETR, UART2_RTS, I2C2_SDA, BTIM2_TOGP, SPI1_SCK, GTIM2_CH1, ATIM_CH1A | ADC_IN5, VC1_CH5, VC2_CH0 |

| Pin number | Pin name (function after reset) | Pin type | I/O structure | Notes | Additional functions | |
|------------|------------------------------------|----------|---------------|-------|--|-----------------------------------|
| LQFP48 | | | | | Digital function | Analog function |
| 16 | PA06 | I/O | TTa | - | GTIM3_CH1, UART2_TXD, VC1_OUT, BTIM2_TOGN, SPI1_MISO, GTIM1_CH1, ATIM_BK | ADC_IN6, VC1_CH6, VC2_CH1 |
| 17 | PA07 | I/O | TTa | - | GTIM4_CH1, UART2_RXD, VC2_OUT, BTIM1_TOGP, SPI1_MOSI, GTIM1_CH2, ATIM_CH1B | ADC_IN7, VC1_CH7, VC2_CH2 |
| 18 | PB00 | I/O | TTa | - | UART2_RXD, UART1_CTS, I2C2_SCL, BTIM1_TOGN, HSI_OUT, GTIM1_CH3, ATIM_CH2B | ADC_IN8 / ExRef, VC2_CH3, LVD_CH2 |
| 19 | PB01 | I/O | TTa | - | UART2_TXD, UART1_RTS, I2C2_SDA, GTIM4_TOGN, BTIM3_TOGP, GTIM1_CH4, ATIM_CH3B | ADC_IN9, VC2_CH4 |
| 20 | PB02 | I/O | TTa | - | UART2_CTS, UART1_TXD, HSE_OUT, GTIM4_TOGP, BTIM3_TOGN, GTIM1_ETR, ATIM_CH1A | ADC_IN10, VC2_CH5 |
| 21 | PB10 | I/O | TTa | - | UART2_RTS, UART1_RXD, I2C1_SCL, I2C2_SCL, SPI2_SCK, GTIM2_CH3, ATIM_CH2A | ADC_IN11, VC2_CH6 |
| 22 | PB11 | I/O | TTa | - | LSI_OUT, GTIM4_ETR, I2C1_SDA, I2C2_SDA, BTIM_ETR, GTIM2_CH4, ATIM_CH3A | ADC_IN12, VC2_CH7, LVD_CH3 |
| 23 | VSS | S | - | - | Ground | |
| 24 | VDD | S | - | - | | |
| 25 | PB12 | I/O | TC | - | GTIM2_TOGN, GTIM4_CH4, LSE_OUT, SPI2_CS, SPI1_CS, GTIM1_TOGN, ATIM_BK | |
| 26 | PB13 | I/O | TC | - | GTIM2_TOGP, GTIM4_CH3, I2C2_SCL, SPI2_SCK, SPI1_SCK, GTIM1_TOGP, ATIM_CH1B | |
| 27 | PB14 | I/O | TC | - | GTIM2_CH1, GTIM4_CH2, I2C2_SDA, SPI2_MISO, SPI1_MISO, RTC_OUT, ATIM_CH2B | |
| 28 | PB15 | I/O | TC | - | GTIM2_CH2, GTIM4_CH1, BTIM2_TOGP, SPI2_MOSI, SPI1_MOSI, RTC_1Hz, ATIM_CH3B | |

| Pin number | Pin name (function after reset) | Pin type | I/O structure | Notes | Additional functions | |
|------------|---------------------------------|----------|---------------|-------|--|-----------------|
| | | | | | Digital function | Analog function |
| LQFP48 | | | | | | |
| 29 | PA08 | I/O | TC | - | UART1_TXD,BTIM2_TOGN, MCO_OUT, LVD_OUT, GTIM3_ETR, ATIM_CH1A | |
| 30 | PA09 | I/O | TC | - | UART3_TXD, UART1_RXD, I2C1_SCL, BTIM1_TOGP, SPI1_CS, GTIM3_CH1, ATIM_CH2A | |
| 31 | PA10 | I/O | TC | - | UART3_RXD, UART1_CTS, I2C1_SDA, BTIM1_TOGN, SPI1_SCK, GTIM3_CH2, ATIM_CH3A | |
| 32 | PA11 | I/O | TC | - | UART3_CTS, UART1_RTS, I2C2_SCL, VC1_OUT, SPI1_MISO, GTIM3_CH3 | |
| 33 | PA12 | I/O | TC | - | UART3_RTS, BTIM_ETR, I2C2_SDA, VC2_OUT, SPI1_MOSI, GTIM3_CH4, ATIM_ETR | |
| 34 | PA13/ SWDIO | I/O | TC | 1 | I2C1_SDA, UART1_RXD, UART2_RXD, I2C2_SCL, IR_OUT | |
| 35 | PF06 | I/O | TC | - | UART3_CTS, GTIM4_TOGN, I2C2_SCL, UART2_CTS, I2C1_SCL, GTIM3_TOGN, BTIM3_TOGP | |
| 36 | PF07 | I/O | TC | - | UART3_RTS, I2C1_SDA, GTIM4_TOGP, UART2_RTS, I2C2_SDA, GTIM3_TOGP, BTIM3_TOGN | |
| 37 | PA14/ SWCLK | I/O | TC | 1 | UART3_TXD, I2C1_SCL, UART1_TXD, UART2_TXD, I2C2_SDA | |
| 38 | PA15 | I/O | TC | - | UART3_RXD, GTIM2_CH1, UART1_RXD, UART2_RXD, SPI1_CS, GTIM2_ETR, ATIM_CH1B | |
| 39 | PB03 | I/O | TC | - | UART3_RTS, GTIM2_CH2, UART1_CTS, UART2_TXD, SPI1_SCK, GTIM1_ETR, ATIM_CH2B | |
| 40 | PB04 | I/O | TC | - | UART3_CTS, GTIM4_ETR, UART1_RTS, UART2_CTS, SPI1_MISO, GTIM1_CH1, ATIM_CH3B | |
| 41 | PB05 | I/O | TC | - | GTIM3_CH4, AWT_ETR, UART2_RTS, SPI1_MOSI, GTIM1_CH2, ATIM_CH1A | |

| Pin number | Pin name (function after reset) | Pin type | I/O structure | Notes | Additional functions | |
|------------|---------------------------------|----------|---------------|-------|---|-----------------|
| | | | | | Digital function | Analog function |
| LQFP48 | | | | | | |
| 42 | PB06 | I/O | TC | - | UART3_TXD, GTIM3_CH3, I2C1_SCL, GTIM4_CH4, SPI2_MOSI, GTIM1_TOGN, ATIM_CH2A | |
| 43 | PB07 | I/O | TC | - | UART3_RXD, GTIM3_CH2, I2C1_SDA, GTIM4_CH3, SPI2_MISO, GTIM1_TOGP, ATIM_CH3A | |
| 44 | PF03/ BOOT | I | B | - | | |
| 45 | PB08 | I/O | TC | - | I2C1_SCL, GTIM3_CH1, UART1_TXD, GTIM4_CH2, SPI2_SCK, GTIM1_CH3, ATIM_ETR | |
| 46 | PB09 | I/O | TC | - | I2C1_SDA, GTIM4_CH1, UART1_RXD, IR_OUT, SPI2_CS, GTIM1_CH4, ATIM_BK | |
| 47 | VSS | S | - | - | Ground | |
| 48 | VDD | S | - | - | Digital power supply | |

Caution 1: Afeter reset, these pins are configured as SWDIO and SWCLK functions, and the internal pull-up resistors are turned on by default.

Table 5-3 Alternate functions selected through GPIOA_AFRy registers for port A

| Pin name | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|------------|-----------|-----------|------------|------------|-----------|-----------|-----------|
| PA00 | UART3_CTS | UART2_CTS | RTC_TAMP | VC1_OUT | SPI2_MISO | GTIM2_CH1 | GTIM2_ETR |
| PA01 | UART3_RTS | UART2_RTS | I2C2_SCL | LVD_OUT | SPI2_MOSI | GTIM2_CH2 | RTC_TAMP |
| PA02 | UART3_TXD | UART2_TXD | I2C2_SDA | VC2_OUT | SPI2_SCK | GTIM2_CH3 | AWT_ETR |
| PA03 | UART3_RXD | UART2_RXD | GTIM2_CH2 | PCLK_OUT | SPI2_CS | GTIM2_CH4 | ATIM_CH3A |
| PA04 | | UART2_CTS | I2C2_SCL | HCLK_OUT | SPI1_CS | GTIM2_ETR | ATIM_CH2A |
| PA05 | GTIM2_ETR | UART2_RTS | I2C2_SDA | BTIM2_TOGP | SPI1_SCK | GTIM2_CH1 | ATIM_CH1A |
| PA06 | GTIM3_CH1 | UART2_TXD | VC1_OUT | BTIM2_TOGN | SPI1_MISO | GTIM1_CH1 | ATIM_BK |
| PA07 | GTIM4_CH1 | UART2_RXD | VC2_OUT | BTIM1_TOGP | SPI1_MOSI | GTIM1_CH2 | ATIM_CH1B |
| PA08 | | UART1_TXD | BTIM2_TOGN | MCO_OUT | LVD_OUT | GTIM3_ETR | ATIM_CH1A |
| PA09 | UART3_TXD | UART1_RXD | I2C1_SCL | BTIM1_TOGP | SPI1_CS | GTIM3_CH1 | ATIM_CH2A |
| PA10 | UART3_RXD | UART1_CTS | I2C1_SDA | BTIM1_TOGN | SPI1_SCK | GTIM3_CH2 | ATIM_CH3A |
| PA11 | UART3_CTS | UART1_RTS | I2C2_SCL | VC1_OUT | SPI1_MISO | GTIM3_CH3 | |
| PA12 | UART3_RTS | BTIM_ETR | I2C2_SDA | VC2_OUT | SPI1_MOSI | GTIM3_CH4 | ATIM_ETR |
| PA13/SWDIO | | I2C1_SDA | UART1_RXD | UART2_RXD | I2C2_SCL | IR_OUT | |
| PA14/SWCLK | UART3_TXD | I2C1_SCL | UART1_TXD | UART2_TXD | I2C2_SDA | | |
| PA15 | UART3_RXD | GTIM2_CH1 | UART1_RXD | UART2_RXD | SPI1_CS | GTIM2_ETR | ATIM_CH1B |

Table 5-4 Alternate functions selected through GPIOB_AFRy registers for port B

| Pin name | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|------------|-----------|------------|------------|------------|------------|-----------|
| PB00 | UART2_RXD | UART1_CTS | I2C2_SCL | BTIM1_TOGN | HSI_OUT | GTIM1_CH3 | ATIM_CH2B |
| PB01 | UART2_TXD | UART1_RTS | I2C2_SDA | GTIM4_TOGN | BTIM3_TOGP | GTIM1_CH4 | ATIM_CH3B |
| PB02 | UART2_CTS | UART1_TXD | HSE_OUT | GTIM4_TOGP | BTIM3_TOGN | GTIM1_ETR | ATIM_CH1A |
| PB03 | UART3_RTS | GTIM2_CH2 | UART1_CTS | UART2_TXD | SPI1_SCK | GTIM1_ETR | ATIM_CH2B |
| PB04 | UART3_CTS | GTIM4_ETR | UART1_RTS | UART2_CTS | SPI1_MISO | GTIM1_CH1 | ATIM_CH3B |
| PB05 | | GTIM3_CH4 | AWT_ETR | UART2_RTS | SPI1_MOSI | GTIM1_CH2 | ATIM_CH1A |
| PB06 | UART3_TXD | GTIM3_CH3 | I2C1_SCL | GTIM4_CH4 | SPI2_MOSI | GTIM1_TOGN | ATIM_CH2A |
| PB07 | UART3_RXD | GTIM3_CH2 | I2C1_SDA | GTIM4_CH3 | SPI2_MISO | GTIM1_TOGP | ATIM_CH3A |
| PB08 | I2C1_SCL | GTIM3_CH1 | UART1_TXD | GTIM4_CH2 | SPI2_SCK | GTIM1_CH3 | ATIM_ETR |
| PB09 | I2C1_SDA | GTIM4_CH1 | UART1_RXD | IR_OUT | SPI2_CS | GTIM1_CH4 | ATIM_BK |
| PB10 | UART2_RTS | UART1_RXD | I2C1_SCL | I2C2_SCL | SPI2_SCK | GTIM2_CH3 | ATIM_CH2A |
| PB11 | LSI_OUT | GTIM4_ETR | I2C1_SDA | I2C2_SDA | BTIM_ETR | GTIM2_CH4 | ATIM_CH3A |
| PB12 | GTIM2_TOGN | GTIM4_CH4 | LSE_OUT | SPI2_CS | SPI1_CS | GTIM1_TOGN | ATIM_BK |
| PB13 | GTIM2_TOGP | GTIM4_CH3 | I2C2_SCL | SPI2_SCK | SPI1_SCK | GTIM1_TOGP | ATIM_CH1B |
| PB14 | GTIM2_CH1 | GTIM4_CH2 | I2C2_SDA | SPI2_MISO | SPI1_MISO | RTC_OUT | ATIM_CH2B |
| PB15 | GTIM2_CH2 | GTIM4_CH1 | BTIM2_TOGP | SPI2_MOSI | SPI1_MOSI | RTC_1Hz | ATIM_CH3B |

Table 5-5 Alternate functions selected through GPIOC_AFRy registers for port C

| Pin name | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|---------|-----------|-----------|------------|-----------|------------|-----------|
| PC13 | PLL_OUT | RTC_1Hz | UART1_CTS | RTC_OUT | BTIM_ETR | GTIM3_ETR | RTC_TAMP |
| PC14 | AWT_ETR | GTIM4_CH4 | UART1_RTS | BTIM2_TOGP | SPI2_MISO | GTIM3_TOGN | GTIM3_CH1 |
| PC15 | HSE_OUT | GTIM4_CH3 | GTIM4_ETR | BTIM2_TOGN | SPI2_MOSI | GTIM3_TOGP | GTIM3_CH2 |

Table 5-6 Alternate functions selected through GPIOF_AFRy registers for port F

| Pin name | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|-----------|-----------|------------|------------|----------|------------|------------|
| PF00 | AWT_ETR | GTIM4_CH2 | I2C1_SDA | BTIM1_TOGP | SPI2_SCK | GTIM2_TOGN | GTIM3_CH3 |
| PF01 | LSE_OUT | GTIM4_CH1 | I2C1_SCL | BTIM1_TOGN | SPI2_CS | GTIM2_TOGP | GTIM3_CH4 |
| PF06 | UART3_CTS | I2C1_SCL | GTIM4_TOGN | UART2_CTS | I2C2_SCL | GTIM3_TOGN | BTIM3_TOGP |
| PF07 | UART3_RTS | I2C1_SDA | GTIM4_TOGP | UART2_RTS | I2C2_SDA | GTIM3_TOGP | BTIM3_TOGN |

6 Address mapping

Figure 6-1 CW32A030 internal address mapping

| | | | | |
|-------------|-----------------------------|------------------|--------------------------|------------|
| 0xFFFF FFFF | RES | | | |
| 0xE0FF FFFF | M0+ peripherals | | | |
| 0xE000 0000 | | | | |
| 0x4800 17FF | RES | A H B | 0x4800 1400- 0x4800 17FF | GPIOF |
| 0x4002 0000 | AHB | | 0x4800 0800- 0x4800 0BFF | GPIOC |
| 0x4001 7FFF | RES | | 0x4800 0400- 0x4800 07FF | GPIOB |
| 0x4001 4000 | APB4 | | 0x4800 0000- 0x4800 03FF | GPIOA |
| 0x4001 0000 | APB3 | | 0x4002 3000- 0x4002 33FF | CRC |
| 0x4000 7FFF | RES | | 0x4002 2000- 0x4002 23FF | FLASH CTRL |
| 0x4000 4000 | APB2 | | 0x4002 0000- 0x4002 03FF | DMA |
| 0x4000 0000 | APB1 | A P B 4 | 0x4001 4C00- 0x4001 4FFF | AWT |
| 0x2000 1FFF | RES | | 0x4001 4800- 0x4001 4BFF | BTIM1/2/3 |
| 0x2000 0000 | SRAM (8KB) | | 0x4001 4400- 0x4001 47FF | GTIM4 |
| 0x0010 09FF | RES | | 0x4001 4000- 0x4001 43FF | GTIM3 |
| 0x0010 0000 | Boot program memory (2.5KB) | A P B 3 | 0x4001 3800- 0x4001 3BFF | UART1 |
| 0x0001 27FF | RES | | 0x4001 3000- 0x4001 33FF | SPI1 |
| 0x0001 2780 | OTP(128B) | | 0x4001 2C00- 0x4001 2FFF | ATIM |
| 0x0000 FFFF | RES | | 0x4001 2800- 0x4001 2BFF | VC/LVD |
| 0x0000 0000 | FLASH(64KB) | | 0x4001 2400- 0x4001 27FF | ADC |
| | | | 0x4001 0000- 0x4001 03FF | SYSCTRL |
| | | A P B 2 | 0x4000 5800- 0x4000 5BFF | I2C2 |
| | | | 0x4000 5400- 0x4000 57FF | I2C1 |
| | | | 0x4000 4800- 0x4000 4BFF | UART3 |
| | | | 0x4000 4400- 0x4000 47FF | UART2 |
| | | A P B 1 | 0x4000 3800- 0x4000 3BFF | SPI2 |
| | | | 0x4000 3000- 0x4000 33FF | IWDT |
| | | | 0x4000 2C00- 0x4000 2FFF | WWDT |
| | | | 0x4000 2800- 0x4000 2BFF | RTC |
| | | | 0x4000 1000- 0x4000 13FF | GTIM2 |
| | | | 0x4000 0400- 0x4000 07FF | GTIM1 |

Table 6-1 CW32A030 peripheral register boundary addresses

| Device or bus | Boundary address | Size | Peripheral |
|---------------------|---------------------------|-------|----------------|
| Main FLASH memory | 0x0000 0000 - 0x0000 FFFF | 64KB | Main FLASH |
| OTP memory | 0x0001 2780 - 0x0001 27FF | 128B | OTP |
| Boot program memory | 0x0010 0000 - 0x0010 09FF | 2.5KB | BootLoader |
| SRAM memory | 0x2000 0000 - 0x2000 1FFF | 8KB | SRAM |
| APB1 peripheral | 0x4000 0400 - 0x4000 07FF | 1KB | GTIM1 |
| | 0x4000 1000 - 0x4000 13FF | 1KB | GTIM2 |
| | 0x4000 2800 - 0x4000 2BFF | 1KB | RTC |
| | 0x4000 2C00 - 0x4000 2FFF | 1KB | WWDT |
| | 0x4000 3000 - 0x4000 33FF | 1KB | IWDT |
| | 0x4000 3800 - 0x4000 3BFF | 1KB | SPI2 |
| APB2 peripheral | 0x4000 4400 - 0x4000 47FF | 1KB | UART2 |
| | 0x4000 4800 - 0x4000 4BFF | 1KB | UART3 |
| | 0x4000 5400 - 0x4000 57FF | 1KB | I2C1 |
| | 0x4000 5800 - 0x4000 5BFF | 1KB | I2C2 |
| APB3 peripheral | 0x4001 0000 - 0x4001 03FF | 1KB | SYSCTRL |
| | 0x4001 2400 - 0x4001 27FF | 1KB | ADC |
| | 0x4001 2800 - 0x4001 2BFF | 1KB | VC/LVD |
| | 0x4001 2C00 - 0x4001 2FFF | 1KB | ATIM |
| | 0x4001 3000 - 0x4001 33FF | 1KB | SPI1 |
| | 0x4001 3800 - 0x4001 3BFF | 1KB | UART1 |
| APB4 peripheral | 0x4001 4000 - 0x4001 43FF | 1KB | GTIM3 |
| | 0x4001 4400 - 0x4001 47FF | 1KB | GTIM4 |
| | 0x4001 4800 - 0x4001 4BFF | 1KB | BTIM1/2/3 |
| | 0x4001 4C00 - 0x4001 4FFF | 1KB | AWT |
| AHB peripheral | 0x4002 0000 - 0x4002 03FF | 1KB | DMA |
| | 0x4002 2000 - 0x4002 23FF | 1KB | FLASH CTRL |
| | 0x4002 3000 - 0x4002 33FF | 1KB | CRC |
| | 0x4800 0000 - 0x4800 03FF | 1KB | GPIOA |
| | 0x4800 0400 - 0x4800 07FF | 1KB | GPIOB |
| | 0x4800 0800 - 0x4800 0BFF | 1KB | GPIOC |
| | 0x4800 1400 - 0x4800 17FF | 1KB | GPIOF |
| M0+ peripheral | 0xE000 0000 - 0xE00F FFFF | 1MB | M0+ peripheral |

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

7.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25^\circ\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\Sigma$).

7.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25^\circ\text{C}$ and $V_{DD} = 3.3\text{V}$. They are given only as design guidelines and are not tested.

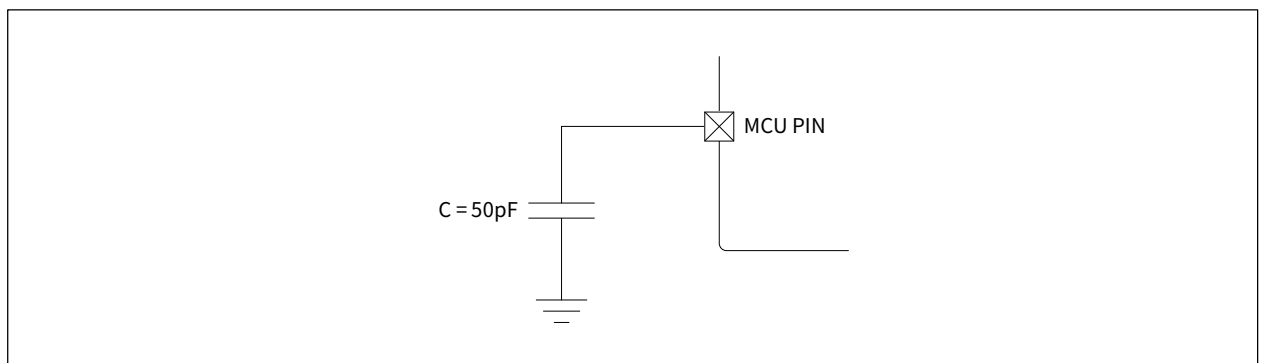
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below:

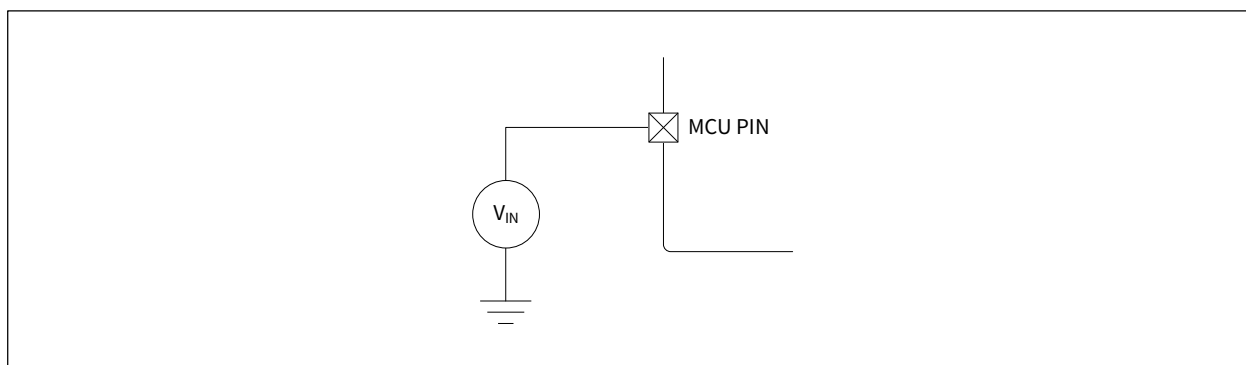
Figure 7-1 Pin loading conditions



7.1.5 Pin input voltage

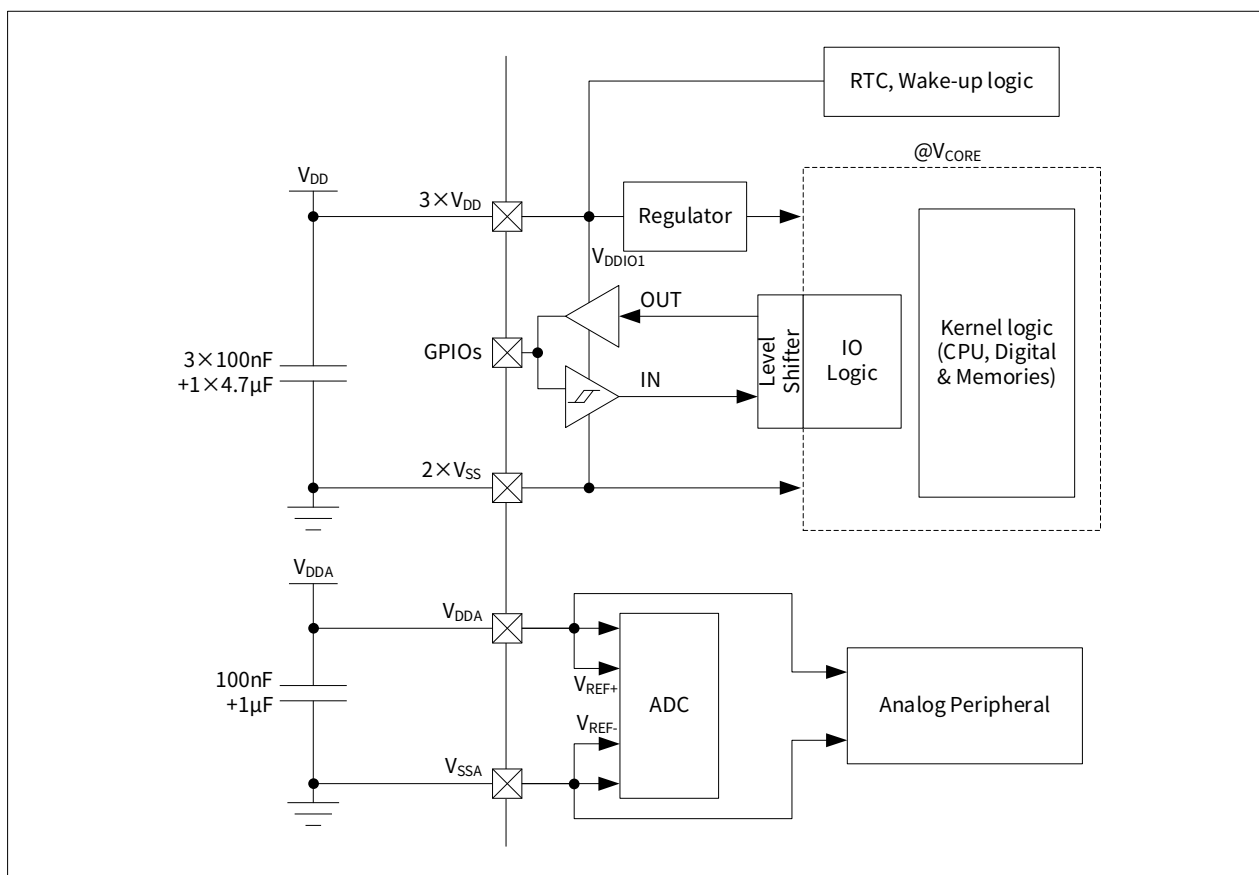
The input voltage measurement on a pin of the device is described in the figure below:

Figure 7-2 Pin input voltage



7.1.6 Power system

Figure 7-3 Power system

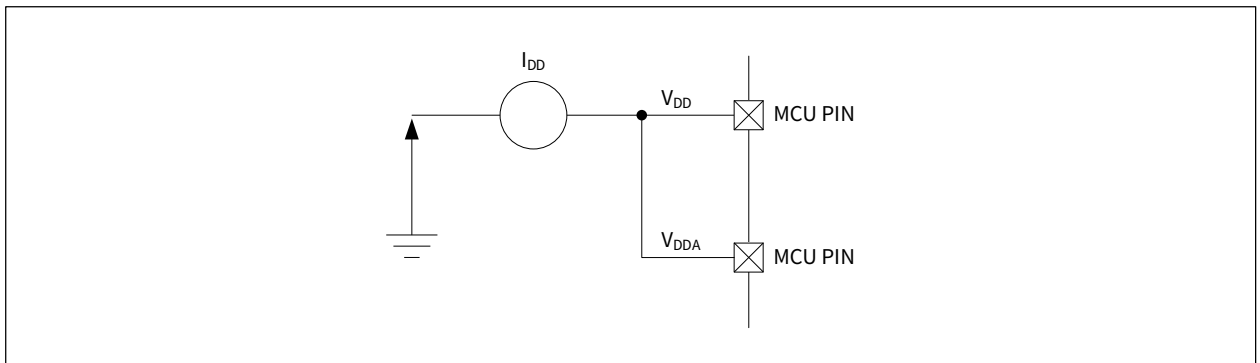


Caution 1: Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Caution 2: All V_{DD} pins must be powered and at the same voltage.

7.1.7 Current consumption measurement

Figure 7-4 Method of measurement



7.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 7-1, Table 7-2 and Table 7-3 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7-1 Voltage characteristics¹

| Symbol | Ratings | Min. | Max. | Unit |
|----------------------|--|--|----------------|------|
| $V_{DD} - V_{SS}$ | External main supply voltage | -0.3 | 6.0 | V |
| $V_{DDA} - V_{SS}$ | External analog supply voltage | -0.3 | 6.0 | V |
| $V_{DD} - V_{DDA}$ | Allowed voltage difference for $V_{DD} > V_{DDA}$ | - | 0.3 | V |
| V_{IN}^2 | Input voltage on port IO | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | V |
| $ \Delta V_{DDx} $ | Variations between all the different V_{DD} pins | - | 0.05 | V |
| $ V_{SSx} - V_{SS} $ | Variations between all the different V_{SS} pins | - | 0.05 | V |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | See Table 7-24 ESD characteristics | | kV |

Caution 1: All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Caution 2: V_{IN} maximum must always be respected, refer to Table 7-2 for the maximum allowable injection current value.

Table 7-2 Current characteristics

| Symbol | Ratings | Max. | Unit |
|--------------------------------|---|----------|------|
| ΣI_{VDD} | Total current into sum of all V_{DD} power lines (source) ¹ | 120 | mA |
| ΣI_{VSS} | Total current out of sum of all V_{SS} power lines (sink) ¹ | -120 | |
| $I_{VDD(PIN)}$ | Total current into sum of a single V_{DD} power lines (source) ¹ | 100 | |
| $I_{VSS(PIN)}$ | Total current out of sum of a single V_{SS} power lines (sink) ¹ | -100 | |
| $I_{IO(PIN)}$ | Current into a single I/O or control pin | +25 | |
| | Current out of a single I/O or control pin | -25 | |
| $\Sigma I_{IO(PIN)}$ | Total output current sunk by sum of all I/Os or control pins | +80 | |
| | Total output current sourced by sum of all I/Os or control pins | -80 | |
| $I_{INJ(PIN)}$ ^{2, 3} | Injected current on TC and RST pins | ± 5 | |
| | Injected current on TTA pins | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins) ⁴ | ± 25 | |

Caution 1: All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Caution 2: $I_{INJ(PIN)}$ must not exceed its limit to ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed to not to exceed its maximum value, also ensure that external limit $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.

Caution 3: Negative injection disturbs the analog performance of the device.

Caution 4: When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents. This result is based on the characterization of the maximum value of $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 Thermal characteristics

| Symbol | Ratings | Value | Unit |
|-----------|------------------------------|-------------|------|
| T_{STG} | Storage temperature range | -65 to +150 | °C |
| T_J | Maximum junction temperature | 125 | |

7.3 Operating conditions

7.3.1 General operating conditions

Table 7-4 General operating conditions

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|-------------------|---|---|------|------------------------|--------------------|
| f_{HCLK} | Internal AHB bus frequency | $V_{\text{DD}} \geq 1.8\text{V}$ | 0 | 64 | MHz |
| f_{PCLK} | Internal APB bus frequency | $V_{\text{DD}} \geq 1.8\text{V}$ | 0 | 64 | |
| f_{HCLK} | Internal AHB bus frequency | $1.65\text{V} \leq V_{\text{DD}} < 1.8\text{V}$ | 0 | 24 | |
| f_{PCLK} | Internal APB bus frequency | $1.65\text{V} \leq V_{\text{DD}} < 1.8\text{V}$ | 0 | 24 | |
| V_{DD} | Standard operating voltage | - | 1.65 | 5.5 | V |
| V_{DDA} | Analog operating voltage | Must be equal to V_{DD} | 1.65 | 5.5 | V |
| V_{IN} | I/O input voltage | TC I/O | -0.3 | $V_{\text{DD}} + 0.3$ | V |
| | | TTa I/O | -0.3 | $V_{\text{DDA}} + 0.3$ | |
| | | BOOT | 0 | $V_{\text{DD}} + 0.3$ | |
| P_{D} | Power dissipation at $T_{\text{A}} = 105^{\circ}\text{C}$ for suffix 7 ¹ | LQFP48 | - | 364 | mW |
| T_{A} | Ambient temperature (suffix 7 version) | Maximum power dissipation | -40 | 105 | $^{\circ}\text{C}$ |
| | | Low power dissipation ² | -40 | 125 | |
| T_{J} | Junction temperature range | Suffix 7 version | -40 | 125 | $^{\circ}\text{C}$ |

Caution 1: If T_{A} is lower, higher P_{D} values are allowed as long as T_{J} does not exceed T_{Jmax} (See 8.6 Thermal characteristics).

Caution 2: In low power dissipation state, T_{A} can be extended to this range as long as T_{J} does not exceed T_{Jmax} (See 8.6 Thermal characteristics).

7.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are tested under the working conditions listed in [Table 7-4 General operating conditions](#).

Table 7-5 Operating conditions at power-up / power-down

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|------------|--------------------------|------------|------|----------|-----------------|
| t_{VDD} | V_{DD} rise time rate | - | 0 | ∞ | $\mu\text{s/V}$ |
| | V_{DD} fall time rate | | 20 | ∞ | |
| t_{VDDA} | V_{DDA} rise time rate | - | 0 | ∞ | |
| | V_{DDA} fall time rate | | 20 | ∞ | |

7.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are tested under the working conditions listed in [Table 7-4 General operating conditions](#).

Table 7-6 Embedded reset and power control block characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|-------------------------------------|--------------|-------------------|------|-------------------|------|
| $V_{POR/BOR}$ | Power on/power down reset threshold | Falling edge | 1.45 ¹ | 1.50 | 1.55 ² | V |
| | | Rising edge | 1.50 ² | 1.55 | 1.60 | V |
| $V_{BORhyst}$ ³ | BOR hysteresis | - | - | 50 | - | mV |
| $t_{RSTTEMPO}$ ³ | Reset temporization | - | 2 | 2.50 | 3 | ms |

Caution 1: The product behavior is guaranteed by design down to the minimum $V_{POR/BOR}$ value.

Caution 2: Data based on characterization results, not tested in production.

Caution 3: Guaranteed by design, not tested in production.

7.3.4 Internal reference voltage

Table 7-7 Internal reference voltage

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------------|--|--|------------------|------|------------------|-------------------------|
| $V_{REFINT1V5}$ | Internal 1.5V reference voltage | $-40^{\circ}\text{C} < T_A < +105^{\circ}\text{C}$ | 1.485 | 1.50 | 1.515 | V |
| $V_{REFINT2V5}$ | Internal 2.5V reference voltage | $-40^{\circ}\text{C} < T_A < +105^{\circ}\text{C}$ | 2.475 | 2.50 | 2.525 | V |
| ΔV_{REFINT} | Internal reference voltage spread over the temperature range | $V_{DDA} = 3\text{V}$ | - | - | 10 ¹ | mV |
| T_{Coeff} | Temperature coefficient | - | -60 ¹ | - | +60 ¹ | ppm/ $^{\circ}\text{C}$ |

Caution 1: Guaranteed by design, not tested in production.

7.3.5 Supply current characteristics

Current consumption is affected by many factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

Figure 7-4 Method of measurement shows the circuit for testing current consumption.

All result of the Run-mode current consumption measurements based on the same limited code used to test CoreMark.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency :
 - 0 wait state inserted when 0 to 24MHz
 - 1 wait state inserted when above 24MHz
 - 2 wait state inserted when above 48MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The data given in Table 7-8 to Table 7-9 are derived from tests performed under the ambient temperature and supply voltage noted in the remarks. For the test conditions, please refer to [Table 7-4 General operating conditions](#).

Table 7-8 Typical and maximum current consumption at $V_{DD} = V_{DDA} = 5.5V$

| Symbol | Parameter | Conditions | f_{HCLK} | All peripherals enabled | | Unit |
|------------|--|---------------------------|------------|-------------------------|---------------------|------|
| | | | | Typ. | Max. ¹ | |
| | | | | | $T_A = 105^\circ C$ | |
| I_{DD}^2 | Supply current in Active mode, code executing from Flash | HSI or HSE clock, PLL on | 64MHz | 13.8 | 15 | mA |
| | | HSI or HSE clock, PLL off | 24MHz | 6.1 | 6.7 | |
| I_{DD}^2 | Supply current in Sleep mode, code executing from Flash or RAM | HSI or HSE clock, PLL off | 24MHz | 6.0 | 6.5 | |

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.

Caution 2: I_{DD} is the total current consumption of V_{DD} and V_{DDA} .

Table 7-9 Typical and maximum current consumption in DeepSleep

| Symbol | Parameter | Conditions | Typ. @ V_{DD} ($V_{DD} = V_{DDA}$) | Max. ¹ | Unit |
|------------|----------------------------------|--|---|---------------------|---------|
| | | | 3.3V | $T_A = 105^\circ C$ | |
| I_{DD}^2 | Supply current in DeepSleep mode | The regulator is in Active mode, all oscillators are off | 20 | 42 | μA |
| | | The regulator is in Active mode, LSE and RTC are on | 22 | 46 | |

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.

Caution 2: I_{DD} is the total current consumption of V_{DD} and V_{DDA} .

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

- I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up resistors values given in [Table 7-25 I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

If the input voltage level of the I/Os is the intermediate voltage level, it will continuously cause the internal Schmitt trigger to flip, resulting in additional random current consumption (although it is small). If it is required to judge the level flip situation in real time, that should configure the I/Os in analog input mode to avoid this.

Caution 1: *Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.*

- I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where:

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load.

V_{DDIOx} is the I/O supply voltage.

f_{SW} is the I/O switching frequency.

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.



The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 7-10 Switching output I/O current consumption

| Symbol | Parameter | Conditions ¹ | I/O toggling frequency (f_{sw}) | Typ. | Unit |
|----------|-------------------------|---|-------------------------------------|------|------|
| I_{SW} | I/O current consumption | $V_{DDIOx} = 3.3V$ $C_{EXT} = 0pF$ $C = C_{INT} + C_{EXT} + C_S$ | 4MHz | 0.18 | mA |
| | | | 8MHz | 0.37 | |
| | | | 16MHz | 0.76 | |
| | | | 24MHz | 1.39 | |
| | | $V_{DDIOx} = 3.3V$ $C_{EXT} = 22pF$ $C = C_{INT} + C_{EXT} + C_S$ | 4MHz | 0.49 | |
| | | | 8MHz | 0.94 | |
| | | | 16MHz | 2.38 | |
| | | | 24MHz | 3.99 | |
| | | $V_{DDIOx} = 3.3V$ $C_{EXT} = 47pF$ $C = C_{INT} + C_{EXT} + C_S$ | 4MHz | 0.81 | |
| | | | 8MHz | 1.7 | |
| | | | 16MHz | 3.67 | |

Caution 1: $C_S = 7pF$ (estimated value).

7.3.6 Wakeup time from low-power mode

The wakeup times given in the table below are tested during the wake-up phase of the HSIOSC.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from DeepSleep mode, SYSCLK takes the default setting: HSI 4 MHz.

All test environments are from ambient temperature and supply voltage conditions summarized in [Table 7-4 General operating conditions](#).

Table 7-11 Low-power mode wakeup timings

| Symbol | Parameter | Conditions | Typ. @ V_{DD} ($V_{DD} = V_{DDA}$) | Max. | Unit |
|---------------|----------------------------|--------------------------|---|------|---------|
| | | | 3.3V | | |
| $t_{WUSLEEP}$ | Wakeup from Sleep mode | - | 4 | - | HCLK |
| t_{WUDEEP} | Wakeup form DeepSleep mode | Regulator in Active mode | 4.0 | 5.0 | μs |

7.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

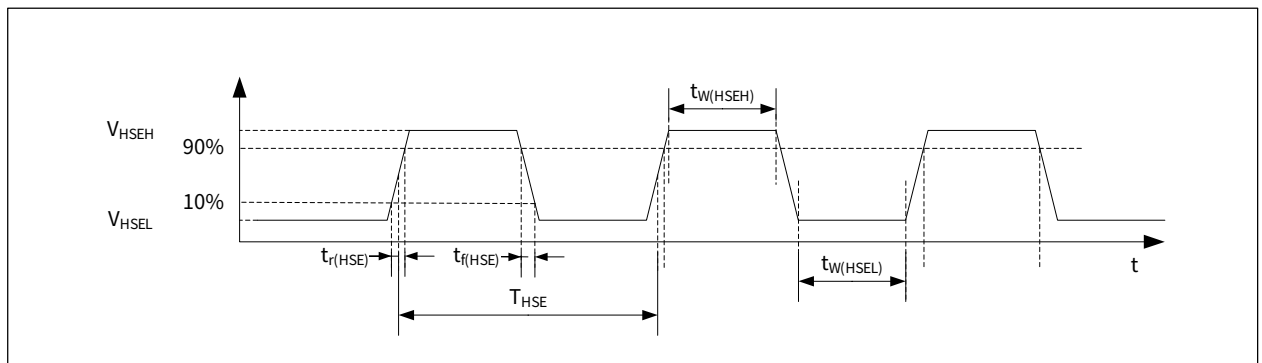
The external clock signal has to respect the I/O characteristics in Section 7.3.12 I/O port characteristics. The recommended clock input waveform is shown in Figure 7-5 High-speed external clock source AC timing diagram.

Table 7-12 High-speed external clock input characteristics

| Symbol | Parameter ¹ | Min. | Typ. | Max. | Unit |
|--------------------------------|--------------------------------------|-----------------|------|-----------------|------|
| f_{HSE_EXT} | User external clock source frequency | 1 | - | 32 | MHz |
| V_{HSEH} | OSC_IN input pin high level voltage | $0.7 V_{DDIOx}$ | - | V_{DDIOx} | V |
| V_{HSEL} | OSC_IN input pin low level voltage | V_{SS} | - | $0.3 V_{DDIOx}$ | |
| $t_{W(HSEH)}$ $t_{W(HSEL)}$ | OSC_IN high or low time | 15 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time | - | - | 20 | |

Caution 1: Guaranteed by design, not tested in production.

Figure 7-5 High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

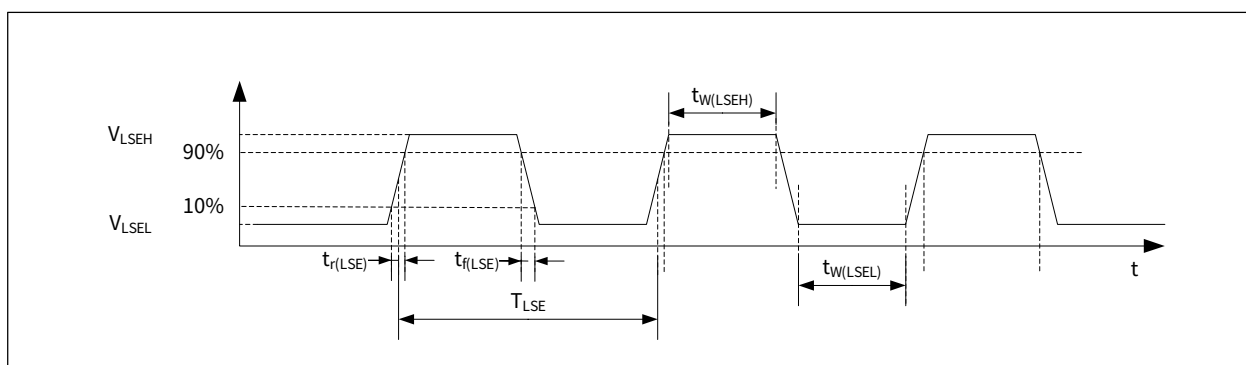
The external clock signal has to respect the I/O characteristics in Section 7.3.12 I/O port characteristics. The recommended clock input waveform is shown in Figure 7-6 Low-speed external clock source AC timing diagram.

Table 7-13 Low-speed external clock input characteristics

| Symbol | Parameter ¹ | Min. | Typ. | Max. | Unit |
|--------------------------------|---------------------------------------|-----------------|--------|-----------------|------|
| f_{LSE_EXT} | User external clock source frequency | - | 32.768 | 1000 | kHz |
| V_{LSEH} | OSC32_IN input pin high level voltage | $0.7 V_{DDIOx}$ | - | V_{DDIOx} | V |
| V_{LSEL} | OSC32_IN input pin low level voltage | V_{SS} | - | $0.3 V_{DDIOx}$ | |
| $t_{W(LSEH)}$ $t_{W(LSEL)}$ | OSC32_IN high or low time | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time | - | - | 50 | |

Caution 1: Guaranteed by design, not tested in production.

Figure 7-6 Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 7-14 HSE oscillator characteristics

| Symbol | Parameter | Conditions ¹ | Min. ² | Typ. | Max. ² | Unit |
|------------------------|-------------------------|--|-------------------|------|-------------------|------|
| $f_{\text{OSC_IN}}$ | Oscillator frequency | - | 4 | 8 | 32 | MHz |
| R_F | Feedback resistor | - | - | 1.4 | - | MΩ |
| I_{DD} | HSE current consumption | During startup ³ | - | - | 900 | μA |
| | | $V_{\text{DD}} = 3.3 \text{ V}$, $R_m = 45 \Omega$, $C_L = 10 \text{ pF@}8 \text{ MHz}$ | - | 430 | - | |
| | | $V_{\text{DD}} = 3.3 \text{ V}$, $R_m = 30 \Omega$, $C_L = 20 \text{ pF@}32 \text{ MHz}$ | - | 980 | - | |
| $t_{\text{su(HSE)}}^4$ | Startup time | V_{DD} is stabilized | - | 2 | - | ms |

Caution 1: Resonator characteristics given by the crystal/ceramic resonator manufacturer.

Caution 2: Guaranteed by design, not tested in production.

Caution 3: This consumption level occurs during the first 2/3 of the $t_{\text{su(HSE)}}$ startup time.

Caution 4: $t_{\text{su(HSE)}}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 7-15 LSE oscillator characteristics ($f_{LSE} = 32.768\text{kHz}$)

| Symbol | Parameter ¹ | Conditions | Min. ¹ | Typ. | Max. ¹ | Unit |
|----------------------------|-------------------------|------------------------------|-------------------|------|-------------------|---------------|
| I_{DD} | LSE current consumption | low drive capability | - | 0.35 | 0.45 | μA |
| | | medium-low drive capability | - | 0.45 | 0.60 | |
| | | medium-high drive capability | - | 0.70 | 0.90 | |
| | | high drive capability | - | 1.60 | 2.00 | |
| $t_{su(LSE)}$ ² | Startup time | V_{DD} stabilized | - | 1.5 | - | s |

Caution 1: Guaranteed by design, not tested in production.

Caution 2: $t_{su(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

7.3.8 Internal clock source characteristics

The data given in the following table is based on the sample tests of the test environment indicated by [Table 7-4 General operating conditions](#).

High-speed internal (HSIOSC) RC oscillator

Table 7-16 HSI oscillator characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|---|------|------|------|---------------|
| f_{HSI} | Frequency | - | - | 48 | - | MHz |
| TRIM | HSI user trimming step | - | - | 0.2 | - | % |
| Duty _{HSI} | Duty cycle | - | 45 | - | 55 | % |
| ACC _{HSI} | Accuracy of the HSI oscillator (factory calibrated) | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | -2.0 | - | +2.0 | % |
| | | $T_A = +25^\circ\text{C}$ | -0.5 | - | +0.5 | % |
| $t_{\text{SU(HSI)}}$ | HSI oscillator startup time | - | 3 | - | 5 | μs |
| $I_{\text{DDA(HSI)}}$ | HSI oscillator power consumption | - | - | 600 | - | μA |

Low-speed internal (LSI) RC oscillator

Table 7-17 LSI oscillator characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|---|------|------|------|---------------|
| f_{LSI} | Frequency | - | - | 32.8 | - | kHz |
| TRIM | LSI user trimming step | - | - | 1 | - | % |
| Duty _{LSI} | Duty cycle | - | 40 | - | 60 | % |
| ACC _{LSI} | Accuracy of the LSI oscillator (factory calibrated) | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | -3 | - | +3 | % |
| | | $T_A = +25^\circ\text{C}$ | -1 | - | +1 | % |
| $t_{\text{SU(LSI)}}$ | LSI oscillator startup time | - | - | - | 50 | μs |
| $I_{\text{DDA(LSI)}}$ | LSI oscillator power consumption | - | - | 1 | - | μA |

Ultra-Low-Speed Internal (RC10K) RC Oscillator

Table 7-18 RC10K oscillator characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|--|---|------|------|------|------|
| f_{RC10K} | Frequency | - | - | 8 | - | kHz |
| Duty _{RC10K} | Duty cycle | - | 45 | - | 55 | % |
| ACC _{RC10K} | Accuracy of the RC10K oscillator(factory calibrated) | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | -50 | - | +50 | % |
| | | $T_A = +25^\circ\text{C}$ | -20 | - | +20 | % |

Mid-low-speed internal (RC150K) RC oscillator

Table 7-19 RC150K oscillator characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------|---|---|------|------|------|------|
| f_{RC150K} | Frequency | - | - | 120 | - | kHz |
| $Duty_{RC150K}$ | Duty cycle | - | 45 | - | 55 | % |
| ACC_{RC150K} | Accuracy of the RC150K oscillator(factory calibrated) | $T_A = -40^{\circ}C \sim +105^{\circ}C$ | -50 | - | +50 | % |
| | | $T_A = +25^{\circ}C$ | -20 | - | +20 | % |

7.3.9 PLL characteristics

The data given in the following table is based on the sample tests of the test environment indicated by [Table 7-4 General operating conditions](#).

Table 7-20 PLL characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------------|-----------------------|------|------|------|---------|
| f_{PLL_IN} | Frequency | 4 | - | 24 | MHz |
| | Duty cycle | 40 | - | 60 | % |
| f_{PLL_OUT} | PLL multiplier output | 8 | - | 64 | MHz |
| t_{LOCK} | PLL lock time | - | 100 | 200 | μs |
| $Jitter_{PLL}$ | Cycle-to-cycle jitter | - | - | 300 | ps |

7.3.10 Memory characteristics

FLASH memory

The characteristics are for 40°C to +105°C test environment unless otherwise specified.

Table 7-21 FLASH memory characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. ¹ | Unit |
|---------------------|-------------------------|---|------|------|-------------------|---------------|
| t_{prog8} | 8-bit programming time | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | - | 31 | - | μs |
| t_{prog16} | 16-bit programming time | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | - | 37 | - | μs |
| t_{prog32} | 32-bit programming time | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | - | 53 | - | μs |
| t_{ERASE} | Page erase time | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | - | 4.5 | - | ms |
| t_{ME} | Mass erase time | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | - | 650 | - | ms |
| I_{DD} | Supply current | Write mode | - | - | 3.5 | mA |
| | | Erase mode | - | - | 2.0 | mA |
| V_{prog} | Programming voltage | - | 1.65 | - | 5.5 | V |

Caution 1: Guaranteed by design, not tested in production.

Table 7-22 FLASH memory endurance and data retention

| Symbol | Parameter | Conditions | Min. ¹ | Unit |
|------------------|----------------|---|-------------------|-------|
| N_{NED} | Endurance | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | 20000 | Times |
| t_{RET} | Data retention | $T_A = 25^\circ\text{C}$ | 100 | Years |
| | | $T_A = 85^\circ\text{C}$ | 25 | |
| | | $T_A = 105^\circ\text{C}$ | 10 | |

Caution 1: Obtained by comprehensive evaluation, not tested in production.

7.3.11 ESD characteristics

Use specific measurement methods to test the strength of the chip to determine its electrical sensitivity performance.

Table 7-23 ESD characteristics

| Symbol | Parameter | Condition | Typ. | Max. | Unit |
|-----------------------|---|---|------|------|------|
| $V_{\text{ESD(HBM)}}$ | Electrostatic discharge voltage (human body model) | $T_A = +25^\circ\text{C}$, conforming to JESD22-A115C | - | 8 | kV |
| $V_{\text{ESD(CDM)}}$ | Electrostatic discharge voltage (charge device model) | $T_A = +25^\circ\text{C}$, conforming to JESD22-A115C | - | 2 | |

7.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by [Table 7-4 General operating conditions](#).

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-24 I/O static characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|------------|------------------------------------|---|-----------------|---------|-----------------|------------|
| V_{IL} | Low level input voltage | TC and TTa I/O | - | - | $0.3 V_{DDIOx}$ | V |
| V_{IH} | High level input voltage | TC and TTa I/O | $0.7 V_{DDIOx}$ | - | - | V |
| V_{hys} | Schmitt trigger hysteresis | TC and TTa I/O | - | 400^1 | - | mV |
| I_{ikg} | Input leakage current | TC and TTa I/O in digital mode $V_{SS} \leq V_{IN} \leq V_{DDIOx}$ | - | - | ± 0.1 | μA |
| | | TTa I/O in digital mode $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$ | - | - | 1 | |
| | | TTa I/O in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$ | - | - | ± 0.2 | |
| R_{PU}^2 | Weak pull-up equivalent resistor | $V_{IN} = V_{SS}$ | 50 | 80 | 180 | k Ω |
| R_{PD}^2 | Weak pull-down equivalent resistor | $V_{IN} = V_{DDIOx}$ | 20 | 30 | 45 | k Ω |
| C_{IO} | I/O pin capacitance | - | - | 5 | - | pF |

Caution 1: Data based on design simulation only. Not tested in production.

Caution 2: Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal.

Output driving current

The GPIOs can sink or source up to $\pm 8\text{mA}$, and sink or source up to $\pm 20\text{mA}$ with a relaxed V_{OH} and V_{OL} .

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section [7.2 Absolute maximum ratings](#):

- The sum of the currents sourced by all the I/Os on V_{DDIOx} , plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 7-1 Voltage characteristics¹](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 7-1 Voltage characteristics¹](#)).

Output voltage levels

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by [Table 7-4 General operating conditions](#).

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-25 Output voltage characteristics

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|-----------|---|----------------------------------|------|------|------|
| V_{OH} | High-level output voltage source current | Sourcing 10mA, $V_{DD} = 3.3V^1$ | 2.37 | - | V |
| V_{OL} | Low-level output voltage sink current | Sinking 15mA, $V_{DD} = 3.3V^1$ | - | 1.10 | |
| V_{OHD} | High-level output voltage dual source current | Sourcing 20mA, $V_{DD} = 3.3V^1$ | 2.37 | - | |
| V_{OLD} | Low-level output voltage dual sink current | Sinking 20mA, $V_{DD} = 3.3V^1$ | - | 0.68 | |

Caution 1: The maximum total current $I_{OH(max)}$ and $I_{OL(max)}$ of all output combinations should not exceed 100mA to meet the maximum specified voltage drop.

Input/output AC characteristics

The values and definitions of the AC characteristics of the I/Os are given by the following charts respectively.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

Table 7-26 I/O AC characteristics

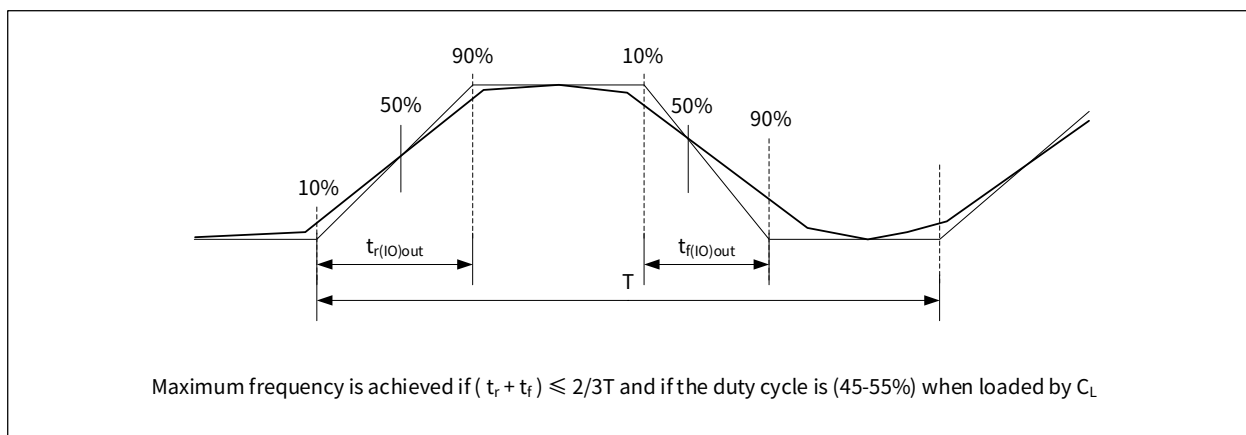
| GPIOx_SPEED.PINy | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|------------------|--------------------|--------------------------------|--|------|------|------|
| 0 | $f_{\max(I/O)out}$ | Maximum frequency ³ | $C_L = 50pF, V_{DDIOx} \geq 2.4V$ | - | 10 | MHz |
| | $t_{f(I/O)out}$ | Output fall time | | - | 25 | ns |
| | $t_{r(I/O)out}$ | Output rise time | | - | 25 | |
| 1 | $f_{\max(I/O)out}$ | Maximum frequency ³ | $C_L = 30pF, V_{DDIOx} \geq 2.7V$ | - | 50 | MHz |
| | | | $C_L = 50pF, V_{DDIOx} \geq 2.7V$ | - | 30 | |
| | | | $C_L = 50pF, 2.4V \leq V_{DDIOx} < 2.7V$ | - | 20 | |
| | $t_{f(I/O)out}$ | Output fall time | $C_L = 30pF, V_{DDIOx} \geq 2.7V$ | - | 5 | ns |
| | | | $C_L = 50pF, V_{DDIOx} \geq 2.7V$ | - | 8 | |
| | | | $C_L = 50pF, 2.4V \leq V_{DDIOx} < 2.7V$ | - | 12 | |
| | $t_{r(I/O)out}$ | Output rise time | $C_L = 30pF, V_{DDIOx} \geq 2.7V$ | - | 5 | |
| | | | $C_L = 50pF, V_{DDIOx} \geq 2.7V$ | - | 8 | |
| | | | $C_L = 50pF, 2.4V \leq V_{DDIOx} < 2.7V$ | - | 12 | |

Caution 1: Data based on design simulation only. Not tested in production.

Caution 2: The speed of the I/O port is determined by the value of the register. For details, please refer to the relevant chapter of the user manual.

Caution 3: The maximum frequency is defined in the figure below.

Figure 7-7 I/O AC characteristics definition



7.3.13 NRST pin characteristics

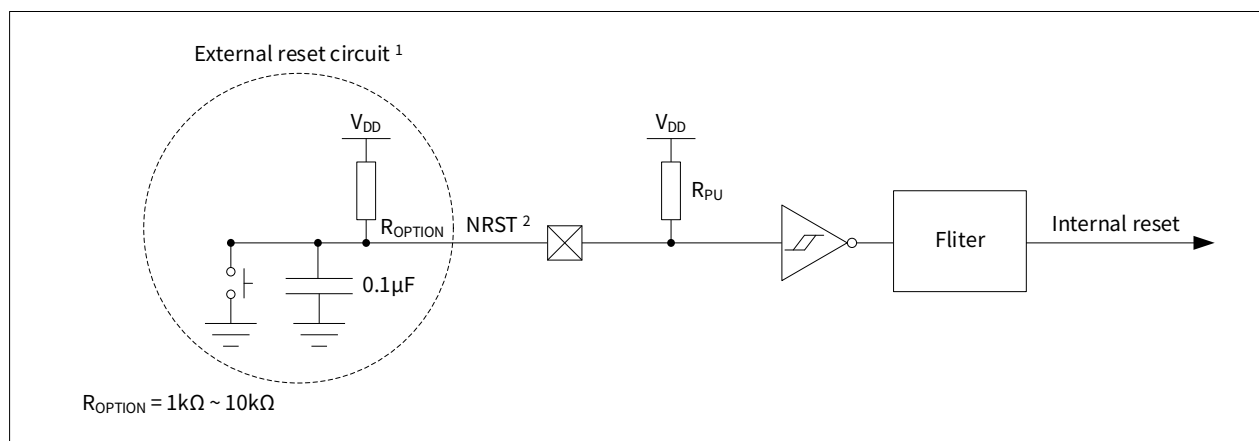
The NRST pin is connected to a permanent pull-up resistor R_{PU} internally.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by [Table 7-4 General operating conditions](#).

Table 7-27 NRST pin characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------|------------------------------------|-------------------|-------------|------|-------------|-----------|
| $V_{IL(NRST)}$ | NRST input low level voltage | - | - | - | $0.3V_{DD}$ | V |
| $V_{IH(NRST)}$ | NRST input high level voltage | - | $0.7V_{DD}$ | - | - | - |
| $V_{hys(NRST)}$ | NRST input voltage hysteresis | - | - | 200 | - | mV |
| R_{PU} | Weak pull-up equivalent resistor | $V_{IN} = V_{SS}$ | 6.3 | 7.3 | 8 | $k\Omega$ |
| $V_{F(NRST)}$ | Minimum required reset pulse width | - | 20 | - | - | μs |

Figure 7-8 Recommended NRST pin protection



Caution 1: The external capacitor protects the device against parasitic resets.

Caution 2: The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 7-28 NRST pin characteristics](#). Otherwise the reset will not be taken into account by the device.

7.3.14 12-bit ADC characteristics

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by [Table 7-4 General operating conditions](#).

Table 7-28 ADC characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------------|---|---------------------------|------|------|-----------|---------------|
| V_{DDA} | Analog supply voltage for ADC ON | - | 1.65 | - | 5.5 | V |
| $I_{DDA(ADC)}$ | Current consumption of the ADC | $V_{DD} = V_{DDA} = 3.3V$ | - | 1.5 | - | mA |
| f_{ADC} | ADC clock frequency | - | - | 24 | - | MHz |
| f_s | Sampling rate | - | - | - | 1 | MHz |
| f_{TRIG} | External trigger frequency | $f_{ADC} = 24MHz$ | - | - | 800 | kHz |
| V_{AIN} | Conversion voltage range | - | 0 | - | V_{DDA} | V |
| R_{AIN} | Input impedance | - | - | - | 100 | k Ω |
| C_{ADC} | Internal sample and hold capacitor | - | - | 9 | - | pF |
| t_s | Sampling time | - | 5 | - | 10 | $1 / f_{ADC}$ |
| t_{STAB} | Stabilization time | - | 19 | | | $1 / f_{ADC}$ |
| t_{CONV} | Total conversion time (including sampling time) | - | 24 | - | 29 | $1 / f_{ADC}$ |

Table 7-29 Accuracy of ADC¹

| Symbol | Parameter | Conditions | Min. | Typ. | Max. ² | Unit |
|--------|----------------------------------|---|------|-----------|-------------------|------|
| ET | Composite error | $f_{ADC} = 24\text{MHz}$, $V_{DDA} = 1.65\text{V} \sim 5.5\text{V}$, $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ | - | ± 2.5 | ± 3.0 | LSB |
| EO | Offset error | | - | ± 1.5 | ± 2.4 | |
| EG | Gain error | | - | ± 2.2 | ± 2.7 | |
| DNL | Differential nonlinearity | | - | ± 0.5 | ± 1.0 | |
| INL | Integral nonlinearity | | - | ± 1.0 | ± 3.0 | dB |
| SINAD | Signal-to-noise ratio distortion | | - | 67 | - | |
| SNR | Signal-to-noise ratio | | - | 66 | - | |
| THD | Total harmonic distortion | - | -70 | - | - | - |
| ENOB | Significant digits | $V_{ref} = V_{DDA}/\text{ExRef}$ 25KSPS@ $V_{DDA} = 1.65\text{V} \sim 1.8\text{V}$ 100KSPS@ $V_{DDA} = 1.8\text{V} \sim 2\text{V}$ 200KSPS@ $V_{DDA} = 2\text{V} \sim 2.4\text{V}$ | - | 10.2 | - | bits |
| | | $V_{ref} = V_{DDA}/\text{ExRef}$ 500KSPS@ $V_{DDA} = 2.4\text{V} \sim 2.7\text{V}$ 1MSPS@ $V_{DDA} = 2.7\text{V} \sim 5.5\text{V}$ | - | 10.8 | - | |
| | | $V_{ref} = \text{Internal } 1.5\text{V}$ reference voltage 100KSPS@ $V_{DDA} = 1.8\text{V} \sim 2\text{V}$ 200KSPS@ $V_{DDA} = 2\text{V} \sim 5.5\text{V}$ | - | 9.7 | - | |
| | | $V_{ref} = \text{Internal } 2.5\text{V}$ reference voltage 200KSPS@ $V_{DDA} = 2.8\text{V} \sim 5.5\text{V}$ | - | 10.0 | - | |

Caution 1 : ADC DC accuracy values are measured after internal calibration;

Avoid injecting reverse current on any analogue input pin as this can degrade the accuracy of conversions performed on another analogue input, it is recommended to add a Schottky diode (between the pin and ground) to the analogue pin where the reverse current will probably be injected;

Better performance can be achieved over restricted V_{DDA} frequency, and temperature ranges.

Caution 2 : Data based on characterization results, not tested in production.

7.3.15 Temperature sensor characteristics

Table 7-30 TS characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------------------|--|------|---------|---------|------------------------|
| T_L | VSENSE linearity with temperature | - | ± 2 | ± 5 | $^{\circ}\text{C}$ |
| Avg_Slope | Average slope | 2.66 | 2.69 | 2.72 | mV/ $^{\circ}\text{C}$ |
| V_{25} | Voltage at 25 $^{\circ}\text{C}$ ($\pm 5^{\circ}\text{C}$) | 0.77 | 0.79 | 0.8 | V |
| t_{START} | TS internal temperature sensor follower settling time | - | - | 45 | μs |
| $t_{\text{S_temp}}$ | ADC sampling time when reading the temperature | 5 | - | - | μs |



7.3.16 Analog voltage comparator characteristics

Table 7-31 Comparator characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. ¹ | Unit |
|---------------|---|--|------|---------|-------------------|------------------|
| V_{DDA} | Analog supply voltage | - | 1.65 | - | 5.5 | V |
| V_{IN} | Comparator input voltage range | - | 0 | - | V_{DDA} | V |
| t_{START} | Startup time | Ultra low speed | - | 10 | 10 | μs |
| | | Low speed | - | 1 | 2 | |
| | | Medium speed | - | 0.5 | 1 | |
| | | High speed | - | 0.1 | 0.25 | |
| t_D | Delay Time | Ultra low speed | - | 10 | 10 | |
| | | Low speed | - | 1 | 2 | |
| | | Medium speed | - | 0.5 | 1 | |
| | | High speed | - | 0.2 | 0.5 | |
| V_{offset} | Offset Error | - | - | ± 3 | ± 10 | mV |
| dThreshold/dt | Threshold voltage temperature coefficient | $V_{DD} = 3.3V$, $-40^{\circ}C < T_A < +105^{\circ}C$, $V_{-} = (n/64) \times V_{ref}$ | - | 40 | 80 | ppm/ $^{\circ}C$ |
| $I_{DD(VC)}$ | Current consumption | Ultra low speed | - | 0.2 | 0.3 | μA |
| | | Low speed | - | 1 | 1.2 | |
| | | Medium speed | - | 8 | 10 | |
| | | High speed | - | 16 | 20 | |
| V_{hys} | Comparator hysteresis | No hysteresis (VCx_CR0.HYS=00) | - | 0 | - | mV |
| | | Low hysteresis (VCx_CR0.HYS=01) | - | 10 | - | |
| | | Medium hysteresis (VCx_CR0.HYS=10) | - | 20 | - | |
| | | High hysteresis (VCx_CR0.HYS=11) | - | 30 | - | |

Caution 1: Data based on characterization results, not production tested.

7.3.17 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to Section [7.3.12 I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 7-32 Timer characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------------|--------------------------------|----------------------|------|------|----------------|--------------|
| $T_{res(TIM)}$ | Timer resolution | - | - | 1 | - | t_{TIMCLK} |
| | | $f_{TIMCLK} = 64MHz$ | - | 15.6 | - | ns |
| f_{EXT} | Timer external clock frequency | - | - | - | $f_{TIMCLK}/2$ | MHz |
| t_{MAX_COUNT} | Maximum period | - | - | - | 65536 | t_{TIMCLK} |

Table 7-33 IWDWT min/max timeout period at 10 kHz (RC10K)

| Frequency division factor | IWDWT_CR.PRS | Min timeout period | Max timeout period | Unit |
|---------------------------|--------------|--------------------|--------------------|------|
| 4 | 0 | 0.417 | 2560 | ms |
| 8 | 1 | 0.834 | 5120 | |
| 16 | 2 | 1.667 | 10240 | |
| 32 | 3 | 3.334 | 20480 | |
| 64 | 4 | 6.667 | 40960 | |
| 128 | 5 | 13.334 | 81920 | |
| 256 | 6 | 26.667 | 163840 | |
| 512 | 7 | 53.334 | 327680 | |

Table 7-34 WWDT min/max timeout period at 64 MHz (PCLK)

| Frequency division factor | Control bit | Min timeout period | Max timeout period | Unit |
|---------------------------|-------------|--------------------|--------------------|------|
| 4096 | 0 | 0.064 | 2.56 | ms |
| 8192 | 1 | 0.128 | 5.12 | |
| 16384 | 2 | 0.256 | 10.24 | |
| 32768 | 3 | 0.512 | 20.48 | |
| 65536 | 4 | 1.024 | 40.96 | |
| 131072 | 5 | 2.048 | 81.92 | |
| 262144 | 6 | 4.096 | 163.82 | |
| 524288 | 7 | 8.192 | 327.68 | |

7.3.18 Communication interfaces

I2C interface characteristics

- The I2C interface meets the I2C-bus specification and the user manual:
 - Standard-mode (Sm): with a bit rate up to 100 kbit/s
 - Fast-mode (Fm) : with a bit rate up to 400 kbit/s
 - Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s
- The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).
- The SDA and SCL I/O requirements are met with the following restrictions:
 - The SDA and SCL I/O pins are not "true" open-drain, maximum input voltage limited by specification.

When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present.

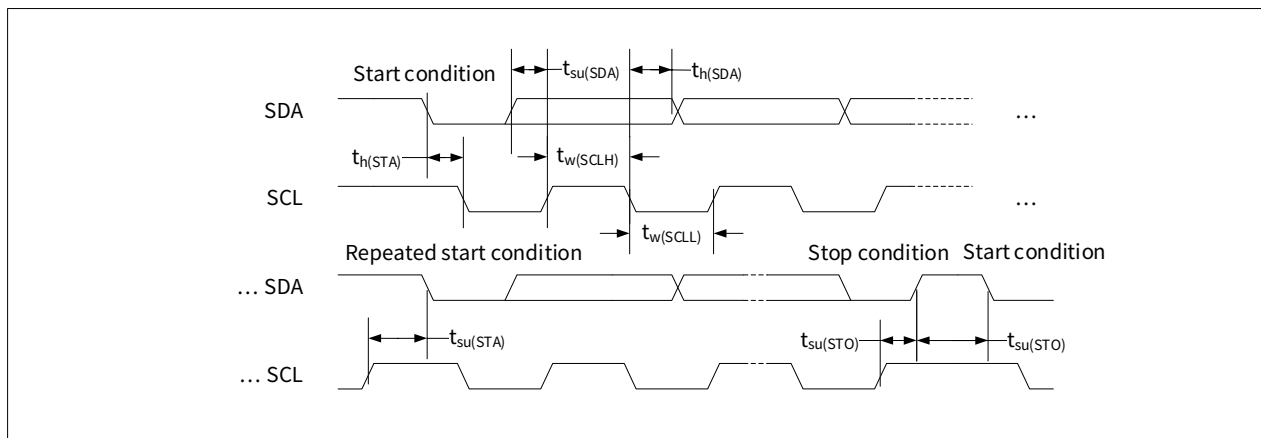
Refer to Section [7.3.12 I/O port characteristics](#) for the I2C I/Os characteristics.

Table 7-35 I2C characteristics

| Symbol | Parameter | Standard mode (100K) | | Fast mode (400K) | | High speed mode (1M) | | Unit |
|------------------|--|----------------------|------|------------------|------|----------------------|------|---------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.25 | - | 0.5 | - | μ s |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | 0.26 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | 50 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | - | 0 | - | 0 | - | |
| $t_{h(STA)}$ | Start condition hold time | 2.5 | - | 0.625 | - | 0.25 | - | μ s |
| $t_{su(STA)}$ | Repeated Start Condition Startup Time | 2.5 | - | 0.6 | - | 0.25 | - | |
| $t_{su(STO)}$ | Stop condition setup time | 0.25 | - | 0.25 | - | 0.25 | - | |
| $t_{w(STO:STA)}$ | Stop condition to start condition time(Bus Idle) | 4.7 | - | 1.3 | - | 0.5 | - | |

Caution 1: Guaranteed by design, not tested in production.

Figure 7-9 I2C timing diagram



SPI interface characteristic parameters

Table 7-36 SPI characteristics

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|------------------------------|-----------------------------|---|-------------------------|------|------|
| $t_{c(SCK)}$ | SPI clock frequency | Master mode $f_{PCLK} \geq 32\text{MHz}$ | 62.5 | - | ns |
| | | Slave mode $f_{PCLK} \geq 48\text{MHz}$ | 83.3 | - | |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | $0.5 \times t_{c(SCK)}$ | - | |
| $t_h(NSS)$ | NSS hold time | Slave mode | $0.5 \times t_{c(SCK)}$ | - | |
| $t_w(SCKH)$ $t_w(SCKL)$ | SCK high and low setup time | Master mode/Slave mode | $0.5 \times t_{c(SCK)}$ | - | |
| $t_{su(MI)}$ $t_{su(SI)}$ | Data input setup time | Master mode | 10 | - | |
| | | Slave mode | 10 | - | |
| $t_h(MI)$ $t_h(SI)$ | Data input hold time | Master mode | 2 | - | |
| | | Slave mode | 2 | - | |
| $t_{v(SO)}$ | Data output valid time | Slave mode $f_{PCLK} = 64\text{MHz}$ | - | 50 | |
| $t_{v(MO)}$ | | Master mode $f_{PCLK} = 32\text{MHz}$ | - | 3 | |
| $t_h(SO)$ | Data output hold time | Slave mode | 30 | - | |
| $t_h(MO)$ | | Master mode $f_{PCLK} = 32\text{MHz}$ | 2 | - | |

Caution 1: Data based on characterization results, not tested in production.

Figure 7-10 SPI timing diagram - slave mode and CPHA=0

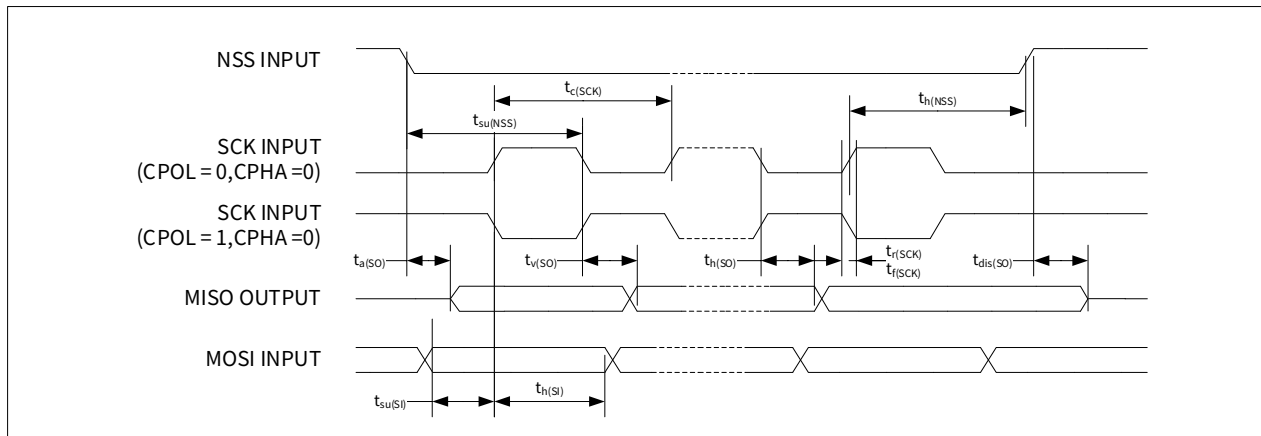


Figure 7-11 SPI timing diagram - slave mode and CPHA=1

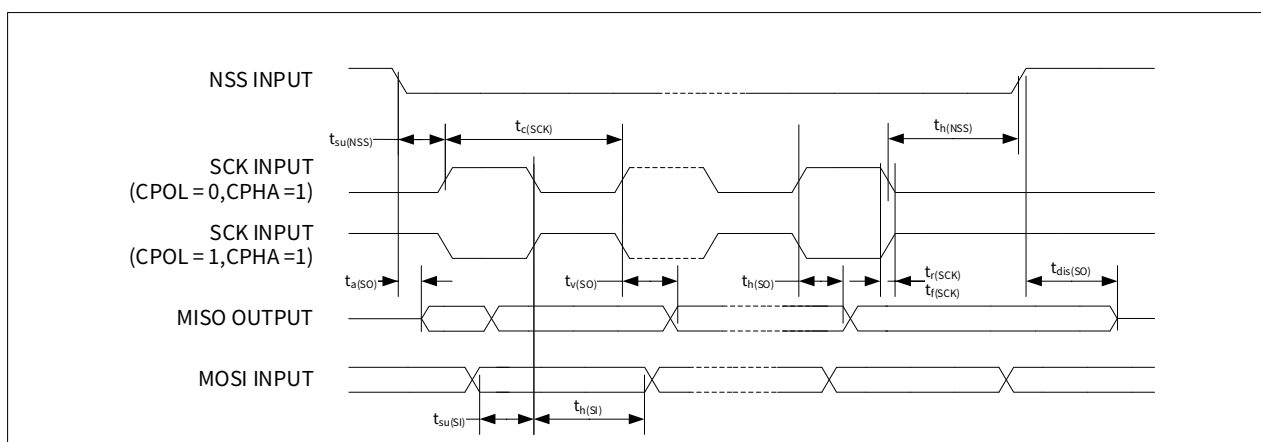
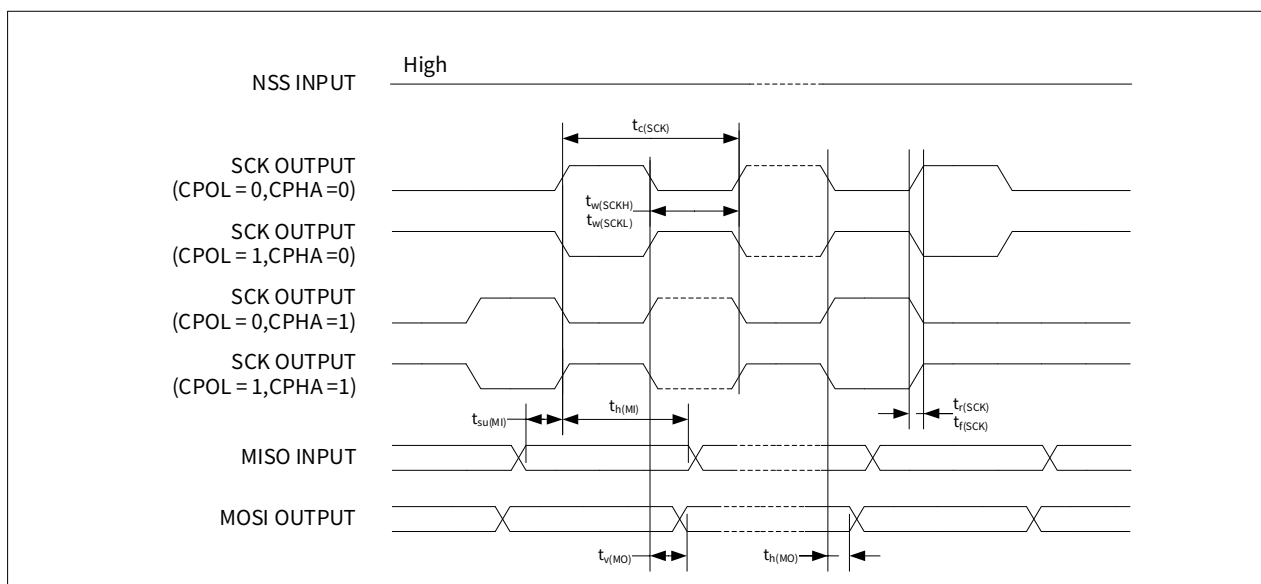


Figure 7-12 SPI timing diagram - master mode

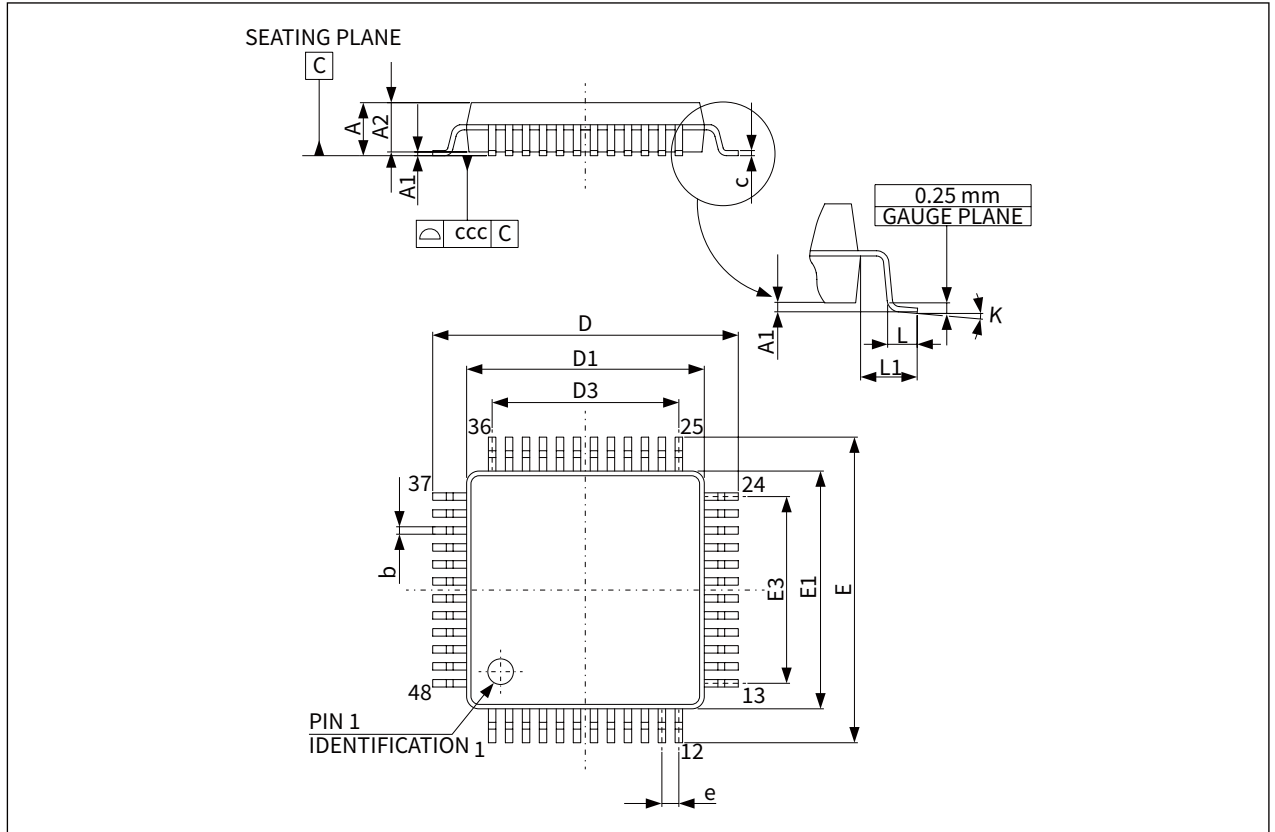


8 Package information

8.1 LQFP48 package information

LQFP48 is 48-pin, 7 x 7mm low-profile quad flat package.

Figure 8-1 LQFP48 outline



Caution 1: Drawing is not to scale.

Table 8-1 LQFP48 mechanical data

| Symbol | Millimeters | | | Inches ¹ | | |
|--------|-------------|-------|-------|---------------------|--------|--------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

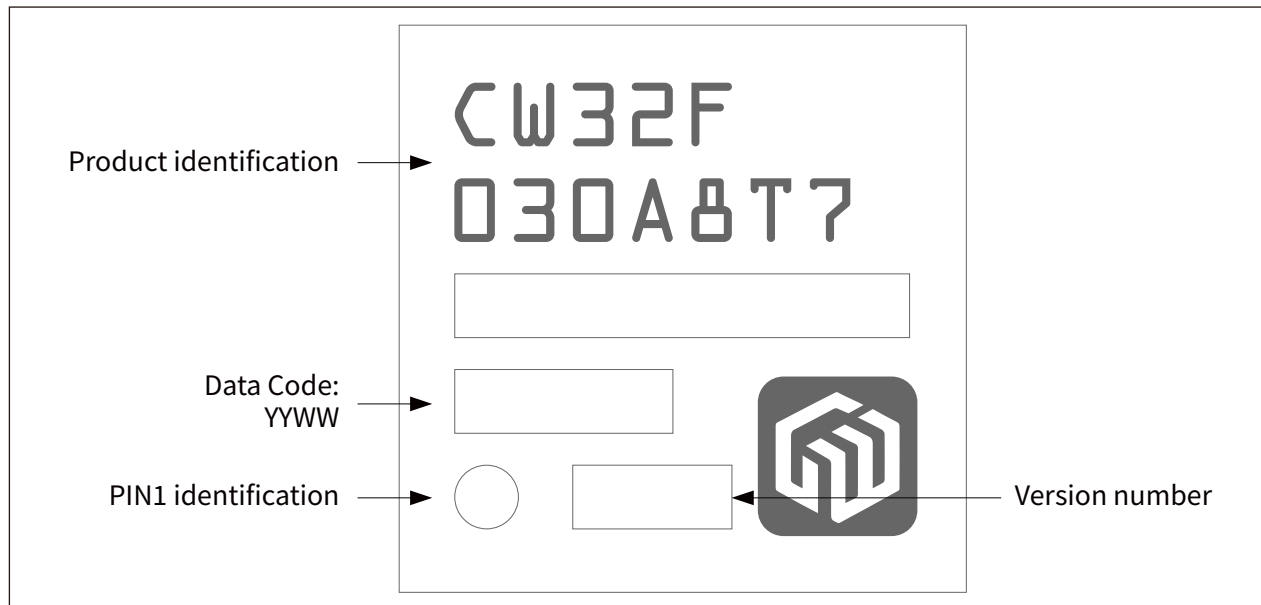
Caution 1: Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-2 LQFP48 topside marking example



Caution 1: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.2 Thermal characteristics

The maximum chip junction temperature T_{Jmax} must never exceed the values given in [Table 7-3 Thermal characteristics](#).

The maximum chip-junction temperature, T_{Jmax} , in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C /W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power
- $P_{I/Omax}$ represents the maximum power dissipation on output pins, where:

$$P_{I/Omax} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DD} - V_{OH}) \times I_{OH})$$

The actual level and current conditions of the I/Os need to be included in the accurate calculation.

Table 8-2 Package thermal characteristics

| Symbol | Parameter | Value | Unit |
|---------------|---|-------|-------|
| Θ_{JA} | Thermal resistance junction-ambient LQFP48 – 7mm X 7mm | 55 | °C /W |

8.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org

9 Ordering information

| | |
|--|------------------------|
| <p>Example:</p> <p><u>Device family</u> CW32=ARM-based</p> <p><u>Product type</u> A=Car Grade</p> <p><u>Sub-family</u> 030=CW32A030xx</p> <p><u>Pin count</u> F=20 pins K=32 pins C=48 pins</p> <p><u>Code size</u> 6=32K字节Flash 8=64K字节Flash</p> <p><u>Package</u> P=TSSOP T=LQFP U/V=QFN</p> <p><u>Temperature range</u> 6=-40°C~85°C 7=-40°C~105°C</p> <p><u>Option</u> xxx=programmed part TR=tape and reel</p> | <h1>CW32A030C8T7x</h1> |
|--|------------------------|

Table 9-1 Minimum Order Quantity (MOQ)

| MCU | Packaging | Quantity | MOQ | MSL | Note |
|--------------|-----------|--------------|----------|-----|---|
| CW32A030C8T7 | Tray | 250 pcs/tray | 2500 pcs | 3 | 10 trays/box, 6 boxes/carton, single box vacuumized |

10 Revision history

Table 10-1 Document revision history

| Date | Revision | Changes |
|-------------------|----------|------------------|
| December 13, 2023 | Rev 1.0 | Initial release. |
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