武汉芯源半导体有限公司
WUHAN XINYUAN SEMICONDUCTOR CO., LTD

CW32W031 Datasheet

ARM® Cortex®-M0+ 32-bit low power wireless MCU, ChirpIoT ™ , with up to 64KB FLASH, 8KB RAM

Rev 1.0

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Contents

1 Features

- Core: ARM® Cortex®-M0+
  - Frequency up to 48 MHz
- Operating temperature: -40°C to 85°C ;
- Operating voltage: 1.8V to 3.6V @ LDO mode ; 2V to 3.6V @ DCDC mode
- Memories
  - Maximum 64 Kbytes FLASH, data retention 25 years @85°C
  - Up to 8 Kbytes RAM, support parity
  - 128 bytes OTP memory
- Radio Frequency
  - Communication band: 370MHz ~ 590MHz, 740MHz ~ 1180MHz
  - Modulation method: ChirpIoT ™
  - Transmission output power: -7dBm ~ 22dBm
  - Maximum link budget: 162dB
  - Receive sensitivity: -140dBm@62.5kHz
  - Operating current

    DeepSleep current: 400nA

    Receive current: 12.5mA@DCDC mode

    Transmit current: 135mA@22dBm, 83mA@18dBm, 25mA@0dBm
  - Support bandwidth: 62.5kHz, 125kHz, 250kHz, 500kHz
  - Support SF factor: 7 ~ 12, automatic spreading factor recognition supported
  - Support code rate: 4/5, 4/6, 4/7, 4/8
  - Support CAD function
  - Low rate mode support: 0.08kbps ~ 20.4kbps
  - Fully integrated frequency synthesizer
- CRC calculation unit
- Reset and power management
  - Low power modes（Sleep，DeepSleep）
  - Power-on/Power down reset（POR/BOR）
  - Programmable low voltage detector（LVD）

- Clock management
  - 32MHz crystal oscillator for RF subsystems
  - 4 to 32 MHz crystal oscillator
  - 32kHz low speed crystal oscillator
  - Internal 48 MHz RC oscillator
  - Internal 32 kHz RC oscillator
  - Internal 10 kHz RC oscillator
  - Internal 150 kHz RC oscillator
  - Clock monitoring system
  - Allow independent shutdown of each peripheral clock
- Up to 33 I/O ports
  - All I/Os support interrupt function
  - All I/Os support interrupt input filtering
- 4-channel DMA controller
- Analog to digital converter
  - 12-bit accuracy, ±1 LSB
  - Up to 1M SPS conversion speed
  - Internel voltage reference
  - Analog watchdog function
  - Internal temperature sensor
- Dual voltage comparator
- Real Time Clock and Calendar
  - Support wakeup from Sleep/DeepSleep mode
- Timers
  - One 16-bit advanced-control timer for six-channel capture/compare and 3 pairs of complementary PWM output, dead time and flexible synchronization function
  - Two groups of 16-bit general-purpose timers
  - Three groups of 16-bit basic timers
  - 16-bit automatic wake-up timer
  - Window watchdog timer
  - Independent watchdog timer
- Communication interfaces
  - Three low-power UARTs with fractional baud rate, support LIN communication interface
  - One SPI interface (12Mbit/s)
  - One I2C interface (1Mbit/s)
  - IR modulator

- Serial wire debug (SWD)
- 80-bit unique ID

Table 1-1 Package model list

Series	Model	Package
CW32W031x8	CW32W031R8	QFN64

2 Introduction

This datasheet provides the ordering information and electromechanical characteristics of the CW32W031 microcontrollers.

This document should be read in conjunction with the CW32W031 reference manual.

For information on the Arm® Cortex®-M0+ core, please refer to the Cortex®-M0+ Technical Reference Manual, available from the *www.arm.com*.

3 Description

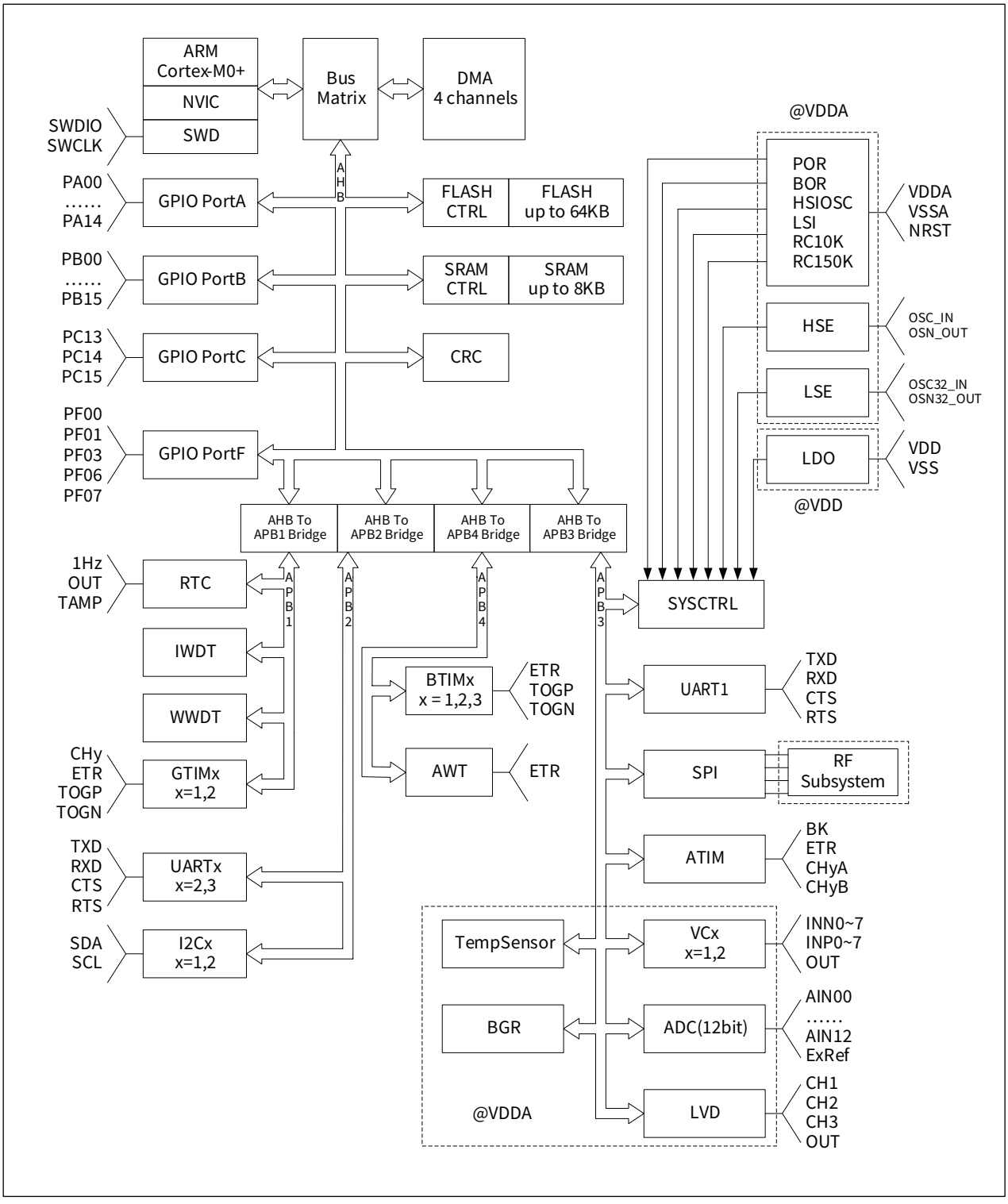
The CW32W031 is a low power long range wireless microcontroller with ChirpIoT ™ modulation technology, supporting half-duplex wireless communication in the 370MHz ~ 590MHz and 740MHz ~ 1180MHz frequency bands.

CW32W031 integrates an ARM® Cortex®-M0+ core with a main frequency up to 48MHz, high-speed embedded memories (up to 64 Kbytes of FLASH and up to 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os.

All devices offer standard communication interfaces (three UARTs, one SPI, one I2C), one 12-bit ADC, five general-purpose and basic timers and an advanced-control PWM timers.

CW32W031 operates in the -40°C to 85°C temperature range from a 1.8 to 3.6V power supply, supports two low-power operating modes (Sleep and DeepSleep). The internal block diagram is shown in the following figure:

Figure 3-1 Internal block diagram



CW32W031 provides QFN64 package, the details of the functions are shown in the following table:

Table 3-1 CW32W031 family device features list

Peripheral		CW32W031R8U6
FLASH（Kbytes）		64
SRAM（Kbytes）		8
ChirpIoT ™		370MHz ~ 590MHz, 740MHz ~ 1180MHz, -7dBm ~ 22dBm
Timers	Advanced control	1
	General purpose	2
	Basic	3
SPI		1
I2C		1
UART		3
12-bit ADC (number of channels)		1 (13 ext. + 3 int.)
GPIO		33
Kernel frequency		48MHz
Operating voltage		LDO mode: 1.8V ~ 3.6V DCDC mode: 2V ~ 3.6V
Operating temperature		-40°C ~ 85°C
Package		QFN64

4 Functional overview

4.1 ARM® Cortex®-M0+ core with embedded Flash and SRAM

The Arm® Cortex®-M0+ processor is the latest generation 32-bit core for small embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The Arm® Cortex®-M0+ 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the small memory.

The CW32W031 family has an embedded Arm core and is therefore compatible with all Arm tools and software.

4.2 Memories

The device has the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for high reliability critical applications.
- The non-volatile memory is divided into two arrays:
  - 64 Kbytes of embedded Flash memory for programs and data
  - 2.5 Kbytes of boot program memory
- FLASH memory erasing and reading protection: The FLASH memory erasing and writing protection is performed through the register, and the 4-level read protection level is set through the ISP command.
  - LEVEL0

    No readout protection, the FLASH memory can be read by SWD or ISP.
  - LEVEL1

    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP or SWD interface. After the downgrade, the FLASH is in the whole chip erasing state.
  - LEVEL2

    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP interface. After the downgrade, the FLASH is in the whole chip erasing state.
  - LEVEL3

    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. Protection level downgrade in any way is not supported.

4.3 Boot mode

At startup, the BOOT pin can be used to select the following two startup options:

- Run the internal bootloader
- Run user program

When running the Bootloader, the user can use the ISP communication protocol for FALSH programming through UART1 (pins are PA13/PA14).

4.4 RF subsystem

4.4.1 ChirpIoT ™ introduction

CW32W031 is embedded with low-power long-range ChirpIoT ™ RF subsystem, operating at 370~590MHz and 740~1180MHz, supporting half-duplex wireless communication, supporting low rate mode from 0.08~20.4kbps, supporting automatic identification of spreading factor and CAD function.

ChirpIoT ™ is a wireless communication modulation and demodulation technology based on a linear spread spectrum signal (Chirp signal). By improving the linear spread spectrum signal in the signal time and frequency domain, it has the following main advantages compared to conventional modulation technologies:

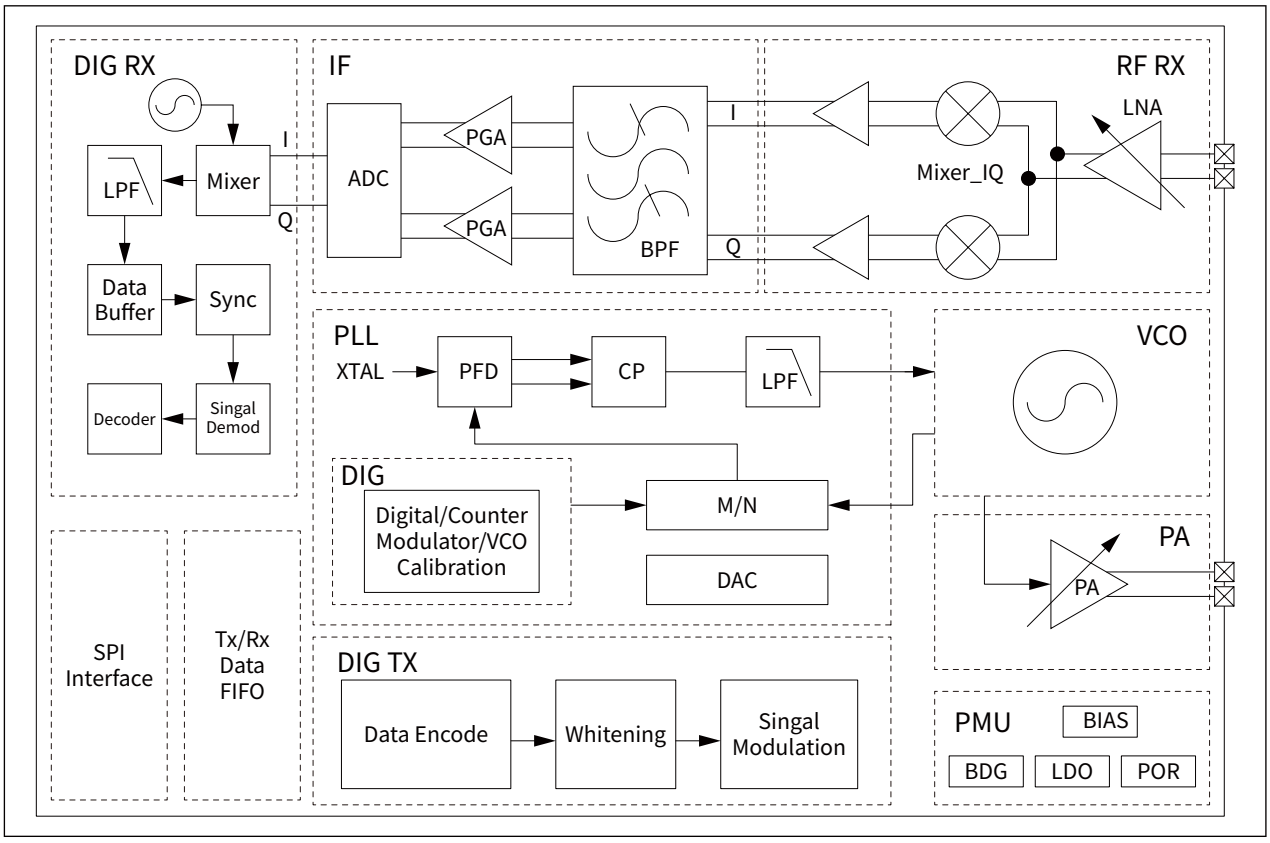
- Significant advantages in blocking and adjacent channel selection, which can further improve communication reliability.
- Greater flexibility for users to adjust the spread spectrum modulation bandwidth, spread factor and error correction rate, effectively improving the trade-off between distance, interference immunity and power consumption for chips using conventional modulation techniques.

The ChirpIoT ™ RF system features high interference immunity, high sensitivity, low power consumption and ultra-long transmission range. With up to -140dBm sensitivity and 22dBm maximum output power, it yields industry-leading link budgets, making it the best choice for long-range transmission and applications where reliability is critical.

4.4.2 RF system block diagram

The RF subsystem integrates RF transmitter, RF receiver, crystal oscillator, frequency generator, power management and ChirpIoT ™ modem functional modules, as shown in the following figure:

Figure 4-1 RF system functional block diagram



4.4.3 RF application reference chart

The RF module contains dedicated pins, please refer to *Table 5-2 CW32W031 pin definitions* for specific pin definitions. The schematics in Figure 4-2, Figure 4-3 and the external components listed in Table 4-1 are for reference only.

Figure 4-2 RF front-end schematic (LDO mode)

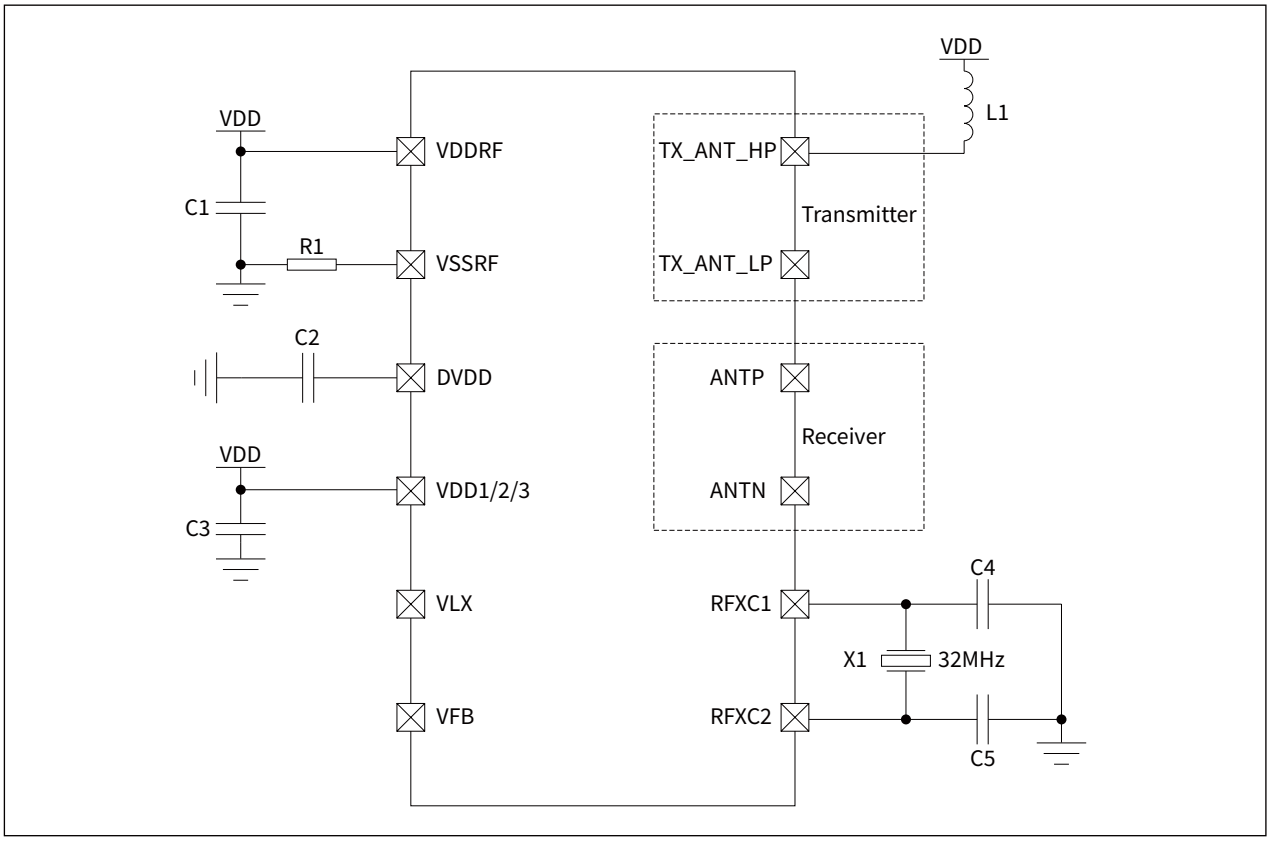


Figure 4-3 RF front-end schematic (DCDC mode)

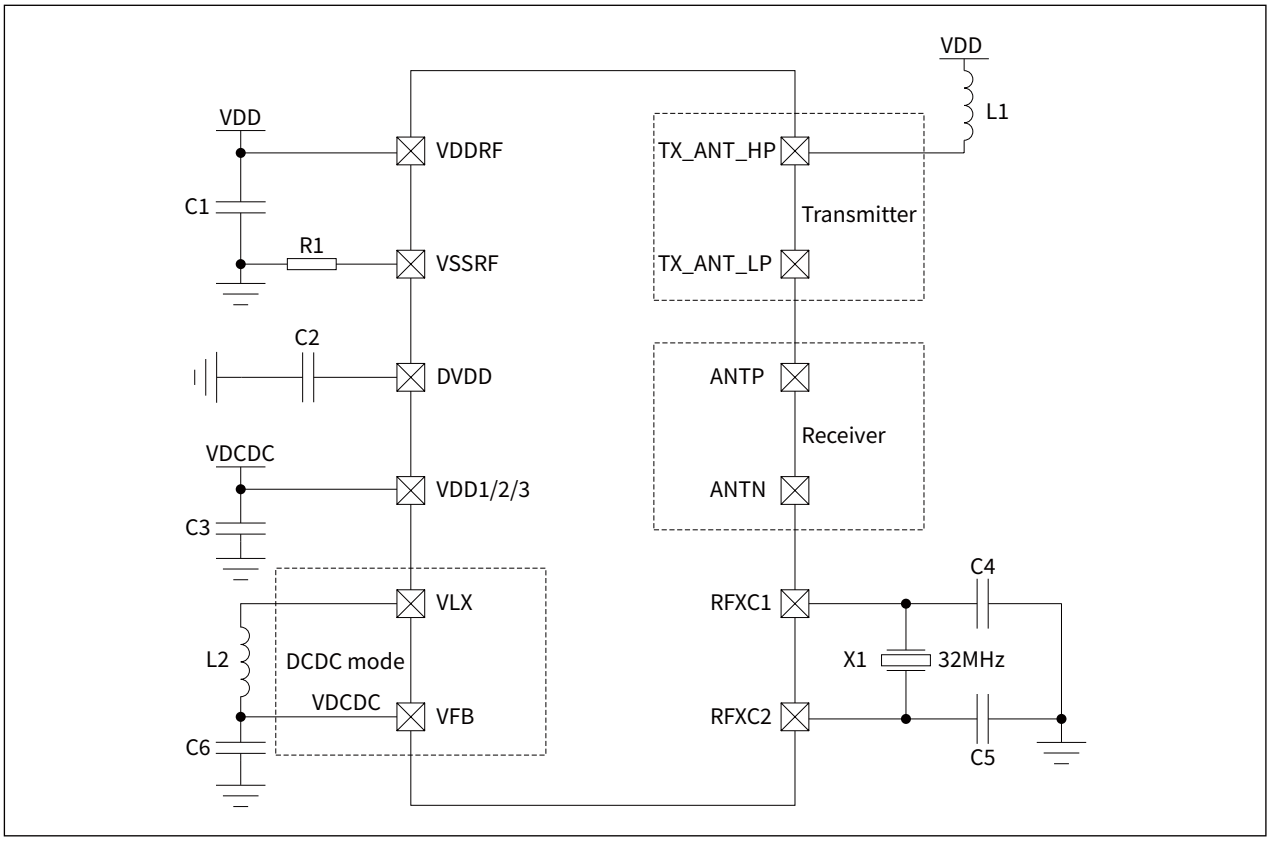


Table 4-1 Typical external components

Component	Description	Value
C1	RF decoupling capacitor	10μF // 3×100nF
R1	Single point grounding	0Ω
C2	Digital power supply LDO output decoupling capacitor	1μF
C3	VDD1/2/3 analogue power supply decoupling capacitor	3×100nF
X1	Crystal[1]	32MHz
C4、C5	Crystal load capacitors	See caution 1
L1	Output bias inductor at the transmitter[2]	See caution 2
L2	DCDC inductor	10μH
C6	DCDC output capacitor	10μF // 10nF

Caution 1: The requirements for external crystals are as follows

1. a crystal frequency of 32 MHz;

2. ESR < 50Ω;

3. Crystal load capacitance ⩽ 12pF;

4. Crystal frequency error ⩽ 10ppm.

Caution 2: The inductor L1 should be adjusted according to the actual RF band, and it is recommended to use devices with DC internal resistance less than 2Ω and rated current greater than 150mA.

4.4.4 RF internal interface

The RF subsystem provides an internal processing unit to handle communication with the CPU. The communication is handled by commands sent through the internal SPI interface and the built-in IRQ interrupt is used to signal events.

The communication interface has been connected internally on the chip, the SPI function on the external pins of the chip is not available when using the RF function and the maximum communication rate required is below 10Mbps.

The RF internal interface pins are shown in the following table:

Table 4-2 RF internal interface

RF interface	Pin
IRQ	PB06
SPI_MOSI	PB05
SPI_MISO	PB04
SPI_CS	PB03
SPI_SCK	PB13

4.5 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit can generate the CRC code of the data stream according to the selected algorithm and parameter configuration.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

The product supports eight commonly used CRC algorithms, including:

CRC16_IBM
CRC16_MAXIM
CRC16_USB
CRC16_MODBUS
CRC16_CCITT
CRC16_CCITT_FALSE
CRC16_X25
CRC16_XMODEM

4.6 Power management

4.6.1 Power supply schemes

- V_{DD} is 1.8V to 3.6V in LDO mode and 2V to 3.6V in DCDC mode
  Provides power to the I/O ports and internal regulator, accessed through the VDD pin.
- V_{DDA} is 1.8V to 3.6V in LDO mode and 2V to 3.6V in DCDC mode
  Power supply for ADC, reset circuit and on-chip RC oscillator, connected through VDDA pin. The V_{DDA} voltage must be always greater or equal to the V_{DD} voltage.
- V_{DDRF} is 1.8V to 3.6V in LDO mode and 2V to 3.6V in DCDC mode
  Power supply for the RF subsystem, connected through the VDDRF pin.
  The VDDRF supplying the RF subsystem is independent, when using the RF subsystem the VDDRF must be connected to the same supply as the VDD.

For details about the power supply, refer to *Figure 7-3 Power system*.

4.6.2 Power supply supervisors

The product integrates power-on reset (POR) and power-down reset (BOR) power monitoring circuits. POR and BOR are always in the working state. When the monitored power supply voltage is lower than a specific voltage threshold ($V_{POR/BOR}$), the chip keeps the reset state without external reset circuit.

The POR/BOR monitors both the VDD and VDDA supply voltages. In order to ensure that the chip works normally after the reset is released, it is necessary to ensure that VDD/VDDA is powered on and off at the same time in the circuit design.

4.6.3 Voltage regulator

The internal voltage regulator has "normal" and "low power" operating modes, and it always enabled after reset.

- The "normal" mode corresponds to a state of full speed operation.
- The "low-power" mode corresponds to some power supply working states, including Sleep and DeepSleep working modes.

4.6.4 Low-power modes

The CW32W031 microcontrollers support two low-power modes:

- Sleep mode
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- DeepSleep mode
  DeepSleep is used to achieve the lowest power consumption, the CPU stops running, the high-speed clock modules (HSE, HSIOSC) are automatically turned off, and the low-speed clocks (LSE, LSI, RC10K, RC150K) remain unchanged.
  The device exits DeepSleep mode when an external reset, or an IWDT reset, or some peripheral interrupts, or an RTC event occurs.

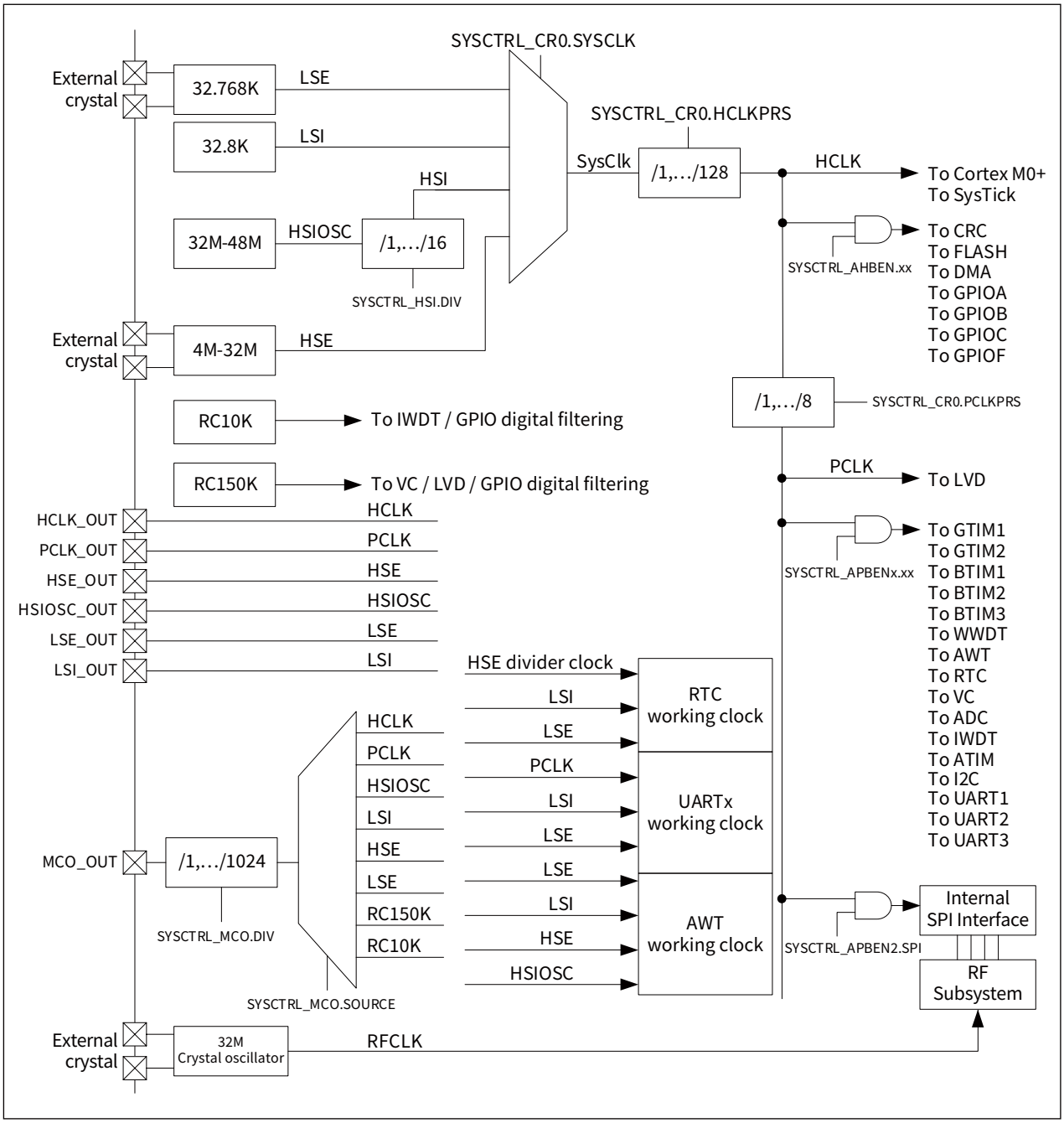
4.7 Clocks and startup

After the MCU is reset, the HSI (generated by the internal 48MHz HSIOSC oscillator frequency division) is selected as the clock source of SysClk by default, and the default value of the system clock frequency is 8MHz.The user can use the program to start the external crystal oscillator and switch the system clock source to the external clock source. The clock failure detection module can continuously detect the state of the external clock source. Once the failure of the external clock source is detected, the system will automatically switch to the internal HSIOSC clock source. If the corresponding fault detection interrupt is enabled, an interrupt will be generated for the user to record fault events.

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

The internal clock tree of the system is shown below :

Figure 4-4 Clock tree of CW32W031



4.8 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Some GPIO pins have analog functions and interface with internal analog peripherals. All I/Os can be configured as external interrupt input pins and have digital filtering.

4.9 Direct memory access controller (DMA)

The chip has a built-in DMA controller, 4 independent channels, high-speed data transmission between peripherals and memory, between peripherals and peripherals, and between memory and memory.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. The software can configure the transmission direction and data length of each channel individually.

4.10 Nested vectored interrupt controller (NVIC)

The CW32W031 family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0+) and supports programmable 4 priority levels.

- Interrupt entry vector table address can be remapped
- Closely coupled NVIC core interface
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved

This hardware block provides flexible interrupt management features with minimal interrupt latency.

4.11 Analog to digital converter (ADC)

The internal 12-bit analog to digital converter has up to 13 external and three internal (temperature sensor, voltage reference measurement, VDDA/3) channels and performs conversions in single-shot or scan modes.

In scan mode, automatic conversion is performed on a selected group of analog inputs.

High-precision voltage reference can be externally connected.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of a selected channel. An interrupt is generated when the converted voltage is outside the programmed thresholds.

4.11.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN14 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of temperature sensor measurement, manufacturers perform individual factory calibrations for each chip. Temperature sensor factory calibration data is stored in FLASH memory.

Table 4-1 Internal temperature sensor calibration value address

ADC reference voltage	Calibration value storage address	Calibration value accuracy
Internal 1.5V	0x0010 0A0A - 0x0010 0A0B	±3°C
Internal 2.5V	0x0010 0A0C - 0x0010 0A0D	±3°C

4.11.2 Internal voltage reference

In addition to VDDA and external reference voltage, ADC reference voltage can also choose internal reference voltage. The internal reference voltage generator (BGR) can provide stable voltage output for ADC, which is 1.5V and 2.5V respectively.

4.12 Analog voltage comparator (VC)

Two analog voltage comparators (VC) are integrated inside, which are used to compare two analog input voltages and output the comparison results from the pins. The positive terminal input of the voltage comparator supports up to 8 external analog inputs, and the negative terminal supports not only 8 external analog inputs, but also internal voltage reference, internal resistance voltage divider, internal temperature sensor and other voltage references. The comparison result output has filtering function, hysteresis window function, and polarity selection. Support compare interrupt, which can be used to wake up MCU in low power mode.

The main features of an analog voltage comparator (VC) are:

- Dual analog voltage comparator VC1、VC2
- Internal 64-step resistor divider
- Up to 8 external analog signal inputs
- 4 on-chip analog input signals
  - Built-in Resistor Divider Output Voltage
  - Built-in temperature sensor output voltage
  - Built-in 1.2V reference voltage
  - ADC reference voltage
- Selectable output polarity
- Support hysteresis window compare function
- Programmable filters and filter times
- 3 interrupt triggering methods, which can be used in combination
  - High level trigger
  - Rising edge trigger
  - Falling edge trigger
- Support running in low power mode, interrupt wake-up MCU

4.13 Low voltage detector (LVD)

Low Voltage Detector (LVD) is used to monitor the VDDA power supply voltage or external pin input voltage. When the comparison results between the monitored voltage and the LVD threshold meets the trigger condition, an LVD interrupt or reset signal will be generated, which is usually used to handle some urgent tasks.

The interrupt and reset flags generated by the LVD can only be cleared by software; only after the interrupt or reset flag is cleared and the trigger condition is reached again, the LVD can generate an interrupt or reset signal again.

The main features of a low voltage detector (LVD) are:

- 4-channel monitoring voltage source: VDDA power supply voltage, PA00, PB00, PB11 pin input
- 16-step threshold voltage, range 1.8V~3.3V
- 3 trigger conditions, which can be used in combination
  - Level Triggered: Voltage Below Threshold
  - Falling edge trigger: the falling edge when the voltage falls below the threshold
  - Rising edge trigger: the rising edge when the voltage rises back above the threshold
- Can trigger to generate interrupt or reset signal, both cannot be generated at the same time
- 8-step filter configurable
- Support hysteresis function
- Support running in low power mode, interrupt wake-up MCU

4.14 Timers and watchdogs

The CW32W031 microcontroller integrates up to two general-purpose timers, three basic timers and one advanced control timer.

The function differences of timers are shown in the following table:

Table 4-2 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	ATIM	16-bit	Up, down, up/down	2^N(N=0,..,7)	YES	6	3
General purpose	GTIM1	16-bit	Up, down, up/down	1,2,3,4,⋯,65536	YES	4	1
	GTIM2	16-bit	Up, down, up/down	1,2,3,4,⋯,65536	YES	4	1
Basic	BTIM1	16-bit	Up	1,2,3,4,⋯,65536	YES	0	1
	BTIM2	16-bit	Up	1,2,3,4,⋯,65536	YES	0	1
	BTIM3	16-bit	Up	1,2,3,4,⋯,65536	YES	0	1

4.14.1 Advanced-control timer (ATIM)

The Advanced-control Timer (ATIM) consists of a 16-bit auto-reload counter and 7 compare units, driven by a programmable prescaler. ATIM supports 6 independent capture/compare channels, which can realize 6 independent PWM outputs or 3 pairs of complementary PWM outputs or capture 6 inputs. Can be used for basic timing/counting, measuring pulse width and period of input signals, generating output waveforms (PWM, single pulse, complementary PWM with dead time inserted, etc.).

4.14.2 General-purpose timers (GTIM1..2)

Two general-purpose timers (GTIMs) are integrated inside. Each GTIM is completely independent and has the same function. Each includes a 16-bit automatic reloading counter and is driven by a programmable prescaler. GTIM supports 4 basic working modes: timer mode, counter mode, trigger start mode and gate control mode. Each group has 4 independent capture/compare channels, which can measure the pulse width of input signals (input capture) or generate output waveforms (output compare and PWM).

4.14.3 Basic timers (BTIM1..3)

Three basic timers (BTIM) are integrated inside, each BTIM is completely independent and has the same function, each contains a 16-bit automatic reloading counter and is driven by a programmable prescaler. BTIM supports four working modes: timer mode, counter mode, trigger start mode and gate control mode, and supports overflow event trigger interrupt request and DMA request. Thanks to the fine processing design of the trigger signal, the BTIM can automatically perform the filtering operation of the trigger signal by the hardware, and can also cause the trigger event to generate interrupts and DMA requests.

4.14.4 Independent watchdog (IWDT)

The Independent Watchdog Timer (IWDT) uses a dedicated internal RC clock source, RC10K, to avoid external influences during operation. Once the IWDT is started, the user needs to reload the counter of the IWDT within a specified time interval, otherwise an overflow will trigger a reset or generate an interrupt signal. After the IWDT is started, the counting can be stopped. The user can choose to keep the IWDT running or suspend counting while in DeepSleep mode.

A specially set key-value register can lock the key registers of the IWDT to prevent the registers from being accidentally modified.

4.14.5 System window watchdog (WWDT)

The CW32W031 microcontroller integrates a window watchdog timer (WWDT), the user needs to refresh within the set time window, otherwise the watchdog overflow will trigger a system reset. WWDT is usually used to monitor the program execution flow with strict time requirements to prevent the abnormal execution of the application program caused by external interference or unknown conditions, resulting in system failure.

4.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0

4.15 Automatic wake-up timer (AWT)

The Automatic Wake-up Timer (AWT) contains a 16bit down counter and is driven by a programmable prescaler. The AWT has a choice of five counting clock sources and can also operate in either timing or counting mode. The AWT can be kept running in deep sleep mode when the counter clock source is LSE or LSI, and a lower overflow interrupt can wake the MCU back to Active mode.

4.16 Real-time clock (RTC)

The Real Time Clock (RTC) is a dedicated counter/timer that provides calendar information including hours, minutes, seconds, date, month, year, and week day.

RTC has two independent alarm clocks, the time and date can be set in combination, and the alarm clock interrupt can be generated and output through the pin; it supports the time stamp function, which can be triggered by the pin, record the current date and time, and generate a time stamp interrupt at the same time; Support periodic interrupt; support automatic wake-up function, which can generate interrupts and output through pins; support 1Hz square wave and RTCOUT output functions; support internal clock calibration compensation.

The CW32W031 has internal independently calibrated RC clock source with a frequency of 32kHz to provide the drive clock for the RTC. The RTC can run in DeepSleep mode and is suitable for applications requiring low power consumption.

4.17 Inter-integrated circuit interfaces (I2C)

The I2C controller can serially send the data to be sent to the I2C bus according to the I2C specification according to the set transmission rate (standard, fast, high-speed), and detect the state during the communication process. I2C also support bus conflict and arbitration handling in multi-master communication.

The main features of the I2C controller are:

- Supports master send/receive and slave send/receive four working modes
- Supports clock stretching (clock synchronization) and multi-master communication collision arbitration
- Supports standard (100Kbps)/fast (400Kbps)/high speed (1Mbps) three working rates
- Supports 7-bit addressing mode
- Supports 3 slave addresses
- Supports broadcast address
- Supports input signal noise filtering function
- Supports interrupt status query function

4.18 Universal asynchronous receiver/transmitter (UART)

Internal integration of three universal asynchronous receiver/transmitter (UART), supports asynchronous full-duplex, synchronous half-duplex and single-wire half-duplex modes, supports hardware data flow control and multi-machine communication, also supports LIN (Local Interconnect Network); The data frame structure is programmable, and a wide range of baud rate selection can be provided through the fractional baud rate generator. Built-in timer module supports wait timeout detection, receive idle detection, automatic baud rate detection and general timing functions.

The UART controller works in a dual clock domain, allowing data reception in DeepSleep mode, and the reception completion interrupt can wake the MCU back to Active mode.

4.19 Serial peripheral interface (SPI)

Serial Peripheral Interface (SPI) supports bidirectional full-duplex, single-wire half-duplex and simplex communication modes, MCU can be configured as master or slave, multi-master communication mode is supported, and direct memory access (DMA) is supported.

The main features of the Serial Peripheral Interface (SPI) are:

- Supports master mode, slave mode
- Supports full-duplex, single-wire half-duplex, simplex
- 4-bit to 16-bit selectable data frame width
- Supports sending and receiving data LSB or MSB first
- Clock Polarity and Clock Phase is programmable
- Communication rates up to PCLK/2 in master mode
- Communication rates up to PCLK/4 in slave mode
- Supports multi-machine communication mode
- 8 interrupt sources with flag bits
- Supports Direct Memory Access (DMA)

4.20 Infrared modulation transmitter (IR)

The built-in infrared modulation transmitter (IR) can be used in conjunction with UART through two general-purpose timers or one general-purpose timer, which can easily implement various standard PWM or PPM encoding methods, and can also realize infrared modulation and transmission of UART data.

The main characteristics of the infrared modulation transmitter (IR) are:

- SIR supporting IrDA Standard 1.0
- Maximum data rate 115.2kbps
- Can adapt to high and low level infrared emission tube

4.21 Serial wire debug port (SWD)

An ARM SWD interface is provided, and users can use the CW-DPLINK of Xinyuan Semiconductor to connect to the MCU to debug and simulate in the IDE development environment.

5 Pin descriptions

Figure 5-1 QFN64 package pinout (top view)

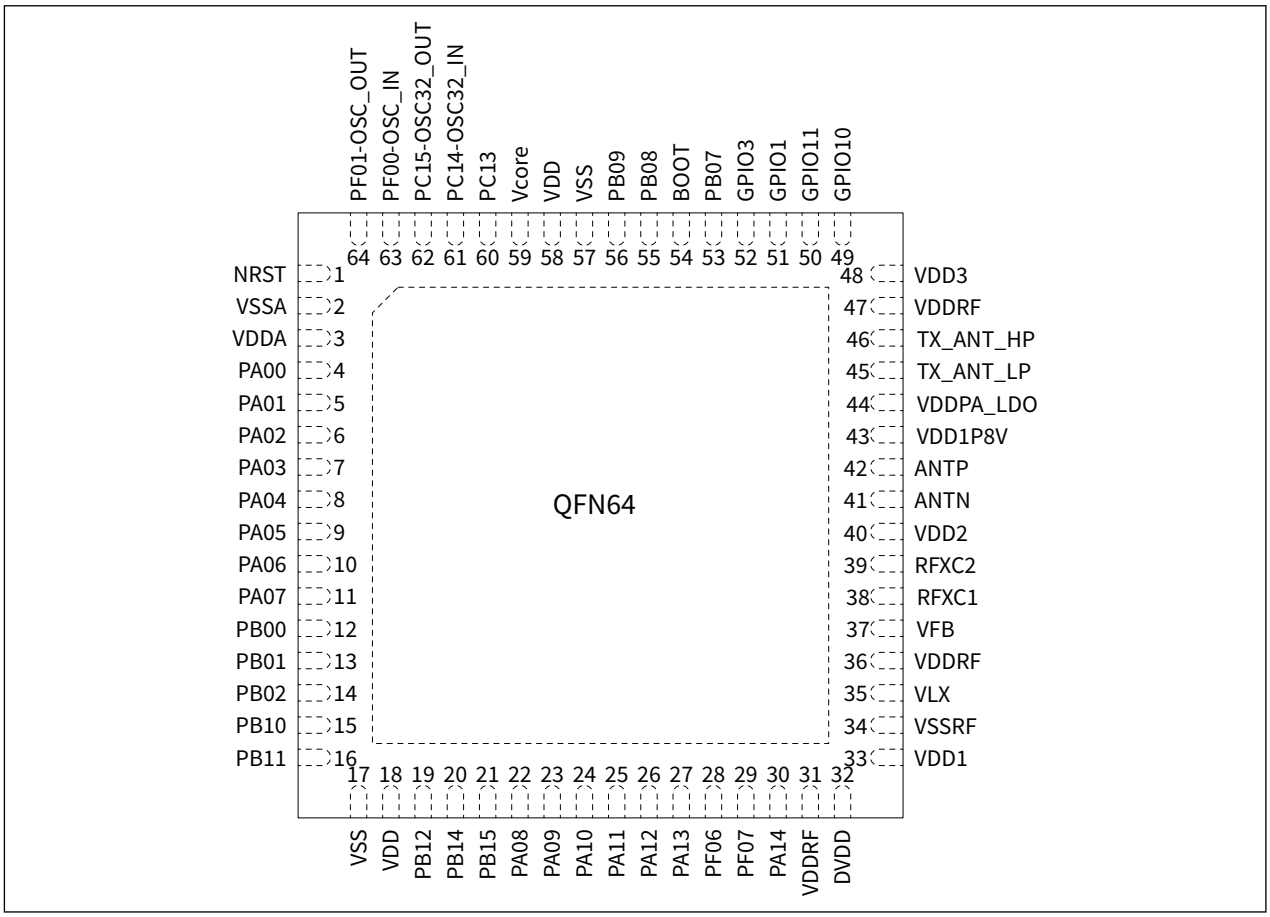


Table 5-1 Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
	O	Output only pin
I/O structure	TTa	Connect the I/O port for the analog function
	TC	Standard I/ O pin
	RF	RF I/O
	B	Dedicated BOOT pin
	RST	Reset input pin
Notes	Unless otherwise specified by a note, all pins are set as high impedance input state after reset	
Additional functions	Digital function	Functions selected through GPIOx_AFRy registers
	Analog function	Functions directly selected through peripheral registers

Table 5-2 CW32W031 pin definitions

Pin number	Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
QFN64					Digital function	Analog function
1	NRST	I	RST	-	Device reset input	
2	VSSA	S	-	-	Analog ground	
3	VDDA	S	-	-	Analog power supply	
4	PA00	I/O	TTa	-	UART3_CTS, UART2_CTS, RTC_TAMP, VC1_OUT, GTIM2_CH1, GTIM2_ETR	ADC_IN0, VC1_CH0, LVD_CH1
5	PA01	I/O	TTa	-	UART3_RTS, UART2_RTS, LVD_OUT, GTIM2_CH2, RTC_TAMP	ADC_IN1, VC1_CH1
6	PA02	I/O	TTa	-	UART3_TXD, UART2_TXD, VC2_OUT, UART3_RXD, GTIM2_CH3, AWT_ETR	ADC_IN2, VC1_CH2
7	PA03	I/O	TTa	-	UART3_RXD, UART2_RXD, GTIM2_CH2, PCLK_OUT, UART3_TXD, GTIM2_CH4, ATIM_CH3A	ADC_IN3, VC1_CH3
8	PA04	I/O	TTa	-	MCO_OUT, UART2_CTS, HCLK_OUT, SPI_CS, GTIM2_ETR, ATIM_CH2A	ADC_IN4, VC1_CH4
9	PA05	I/O	TTa	-	GTIM2_ETR, UART2_RTS, BTIM2_TOGN, SPI_SCK, GTIM2_CH1, ATIM_CH1A	ADC_IN5, VC1_CH5, VC2_CH0
10	PA06	I/O	TTa	-	UART2_RXD, UART2_TXD, VC1_OUT, BTIM2_TOGP, SPI_MISO, GTIM1_CH1, ATIM_BK	ADC_IN6, VC1_CH6, VC2_CH1
11	PA07	I/O	TTa	-	UART2_TXD, UART2_RXD, VC2_OUT, BTIM1_TOGN, SPI_MOSI, GTIM1_CH2, ATIM_CH1B	ADC_IN7, VC1_CH7, VC2_CH2
12	PB00	I/O	TTa	-	UART2_RXD, UART1_CTS, UART2_TXD, BTIM1_TOGP, HSIOSC_OUT, GTIM1_CH3, ATIM_CH2B	ADC_IN8/ ExRef, VC2_CH3, LVD_CH2
13	PB01	I/O	TTa	-	UART2_TXD, UART1_RTS, UART2_RXD, BTIM3_TOGN, GTIM1_CH4, ATIM_CH3B	ADC_IN9, VC2_CH4
14	PB02	I/O	TTa	-	UART2_CTS, UART1_TXD, HSE_OUT, UART1_RXD, BTIM3_TOGP, GTIM1_ETR, ATIM_CH1A	ADC_IN10, VC2_CH5

Pin number	Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
QFN64					Digital function	Analog function
15	PB10	I/O	TTa	-	UART2_RTS, UART1_RXD, I2C_SCL, UART1_TXD, GTIM2_CH3, ATIM_CH2A	ADC_IN11, VC2_CH6
16	PB11	I/O	TTa	-	LSI_OUT, I2C_SDA, BTIM_ETR, GTIM2_CH4, ATIM_CH3A	ADC_IN12, VC2_CH7, LVD_CH3
17	VSS	S	-	-	Digital ground	
18	VDD	S	-	-	Digital power supply	
19	PB12	I/O	TC	-	GTIM2_TOGP, LSE_OUT, SPI_CS, GTIM1_TOGP, ATIM_BK	
20	PB14	I/O	TC	-	GTIM2_CH1, SPI_MISO, RTC_OUT, ATIM_CH2B	
21	PB15	I/O	TC	-	GTIM2_CH2, BTIM2_TOGN, SPI_MOSI, RTC_1Hz, ATIM_CH3B	
22	PA08	I/O	TC	-	UART1_RXD, UART1_TXD, BTIM2_TOGP, MCO_OUT, LVD_OUT, ATIM_CH1A	
23	PA09	I/O	TC	-	UART3_TXD, UART1_RXD, I2C_SCL, BTIM1_TOGN, SPI_CS, UART3_RXD, ATIM_CH2A	
24	PA10	I/O	TC	-	UART3_RXD, UART1_CTS, I2C_SDA, BTIM1_TOGP, SPI_SCK, UART3_TXD, ATIM_CH3A	
25	PA11	I/O	TC	-	UART3_CTS, UART1_RTS, VC1_OUT, SPI_MISO, ATIM_GATE	
26	PA12	I/O	TC	-	UART3_RTS, BTIM_ETR, VC2_OUT, SPI_MOSI, ATIM_ETR	
27	PA13/ SWDIO	I/O	TC	1	I2C_SDA, UART1_RXD, UART2_TXD, IR_OUT	
28	PF06	I/O	TC	-	UART3_CTS, I2C_SCL, UART2_CTS, BTIM3_TOGN	
29	PF07	I/O	TC	-	UART3_RTS, I2C_SDA, UART2_RTS, BTIM3_TOGP	
30	PA14/ SWCLK	I/O	TC	1	UART3_TXD, I2C_SCL, UART1_TXD, UART2_RXD,	
31	VDDRF	S	-	-	Power supply (RF)	

Pin number	Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
QFN64					Digital function	Analog function
32	DVDD	S	-	-	Digital power supply LDO output	
33	VDD1	S	-	-	Analog power supply, DCDC mode connected to VFB, LDO mode connected to main power	
34	VSSRF	S	-	-	Ground (RF)	
35	VLX	-	-	-	Internal DCDC output, DCDC mode connected to external series inductor, LDO mode NC	
36	VDDRF	S	-	-	Power supply (RF)	
37	VFB	-	-	-	Internal DCDC feedback input, DCDC mode connected to VDD1/2/3, LDO mode NC	
38	RFXC1	I	RF	-	32MHz crystal input (RF)	
39	RFXC2	O	RF	-	32MHz crystal output (RF)	
40	VDD2	S	-	-	Analog power supply, DCDC mode connected to VFB, LDO mode connected to main power	
41	ANTN	I	RF	-	Receiving end antenna negative	
42	ANTP	I	RF	-	Receiving end antenna positive	
43	VDD1P8V	S	-	-	Low power PA LDO supply, DCDC mode connected to VFB, LDO mode connected to main power	
44	VDDPA_LDO	S	-	-	Low power LDO output	
45	TX_ANT_LP	O	RF	-	Low power PA output at the transmitting end	
46	TX_ANT_HP	O	RF	-	High power PA output at the transmitting end	
47	VDDRF	S	-	-	Power supply (RF)	
48	VDD3	S	-	-	Analog power supply, DCDC mode connected to VFB, LDO mode connected to main power	
49	GPIO10	I	-	-	RF digital signal input	
		O			RF external PA enable control signal	
50	GPIO11	I	-	-	RF digital IO	
		O			RF channel status indicator signal	
51	GPIO1	I/O	-	-	RF digital IO	

Pin number	Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
QFN64					Digital function	Analog function
52	GPIO3	I/O	-	-	RF digital IO	
53	PB07	I/O	TC	-	UART3_RXD,UART3_TXD, I2C_SDA, GTIM1_TOGN, ATIM_CH3A	
54	PF03/ BOOT	I	B	-		
55	PB08	I/O	TC	-	I2C_SCL, UART1_RXD, UART1_TXD, GTIM1_CH3, ATIM_ETR	
56	PB09	I/O	TC	-	I2C_SDA, UART1_TXD, UART1_RXD, IR_OUT, GTIM1_CH4, ATIM_BK	
57	VSS	S	-	-	Digital ground	
58	VDD	S	-	-	Digital power supply	
59	Vcore	-	-	-	Vcore is the regulator supply output and must be connected to a 1μF capacitor to ground and is for internal circuit use only.	
60	PC13	I/O	TC	-	UART1_TXD, RTC_1Hz, UART1_CTS, RTC_OUT, BTIM_ETR, RTC_TAMP	
61	PC14	I/O	TC	-	AWT_ETR, UART2_TXD, UART1_RTS, BTIM2_TOGN, UART2_RXD	OSC32_IN
62	PC15	I/O	TC	-	HSE_OUT, UART2_RXD, MCO_OUT, BTIM2_TOGP, UART2_TXD, UART1_RXD	OSC32_OUT
63	PF00	I/O	TC	-	AWT_ETR, UART3_TXD, I2C_SDA, BTIM1_TOGN, UART3_RXD, GTIM2_TOGP	OSC_IN
64	PF01	I/O	TC	-	LSE_OUT, UART3_RXD, I2C_SCL, BTIM1_TOGP, UART3_TXD, GTIM2_TOGN	OSC_OUT

Caution 1: Afeter reset，these pins are configured as SWDIO and SWCLK functions，and the internal pull-up resistors are turned on by default.

Table 5-3 Alternate functions selected through GPIOA_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA00	UART3_CTS	UART2_CTS	RTC_TAMP	VC1_OUT		GTIM2_CH1	GTIM2_ETR
PA01	UART3_RTS	UART2_RTS		LVD_OUT		GTIM2_CH2	RTC_TAMP
PA02	UART3_TXD	UART2_TXD		VC2_OUT	UART3_RXD	GTIM2_CH3	AWT_ETR
PA03	UART3_RXD	UART2_RXD	GTIM2_CH2	PCLK_OUT	UART3_TXD	GTIM2_CH4	ATIM_CH3A
PA04	MCO_OUT	UART2_CTS		HCLK_OUT	SPI_CS	GTIM2_ETR	ATIM_CH2A
PA05	GTIM2_ETR	UART2_RTS		BTIM2_TOGN	SPI_SCK	GTIM2_CH1	ATIM_CH1A
PA06	UART2_RXD	UART2_TXD	VC1_OUT	BTIM2_TOGP	SPI_MISO	GTIM1_CH1	ATIM_BK
PA07	UART2_TXD	UART2_RXD	VC2_OUT	BTIM1_TOGN	SPI_MOSI	GTIM1_CH2	ATIM_CH1B
PA08	UART1_RXD	UART1_TXD	BTIM2_TOGP	MCO_OUT	LVD_OUT		ATIM_CH1A
PA09	UART3_TXD	UART1_RXD	I2C_SCL	BTIM1_TOGN	SPI_CS	UART3_RXD	ATIM_CH2A
PA10	UART3_RXD	UART1_CTS	I2C_SDA	BTIM1_TOGP	SPI_SCK	UART3_TXD	ATIM_CH3A
PA11	UART3_CTS	UART1_RTS		VC1_OUT	SPI_MISO		
PA12	UART3_RTS	BTIM_ETR		VC2_OUT	SPI_MOSI		ATIM_ETR
PA13/ SWDIO		I2C_SDA	UART1_RXD	UART2_TXD		IR_OUT	
PA14/ SWCLK	UART3_TXD	I2C_SCL	UART1_TXD	UART2_RXD			

Table 5-4 Alternate functions selected through GPIOB_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB00	UART2_RXD	UART1_CTS	UART2_TXD	BTIM1_TOGP	HSIOSC_OUT	GTIM1_CH3	ATIM_CH2B
PB01	UART2_TXD	UART1_RTS	UART2_RXD		BTIM3_TOGN	GTIM1_CH4	ATIM_CH3B
PB02	UART2_CTS	UART1_TXD	HSE_OUT	UART1_RXD	BTIM3_TOGP	GTIM1_ETR	ATIM_CH1A
PB07	UART3_RXD	UART3_TXD	I2C_SDA			GTIM1_TOGN	ATIM_CH3A
PB08	I2C_SCL	UART1_RXD	UART1_TXD			GTIM1_CH3	ATIM_ETR
PB09	I2C_SDA	UART1_TXD	UART1_RXD	IR_OUT		GTIM1_CH4	ATIM_BK
PB10	UART2_RTS	UART1_RXD	I2C_SCL	UART1_TXD		GTIM2_CH3	ATIM_CH2A
PB11	LSI_OUT		I2C_SDA		BTIM_ETR	GTIM2_CH4	ATIM_CH3A
PB12	GTIM2_TOGP		LSE_OUT		SPI_CS	GTIM1_TOGP	ATIM_BK
PB14	GTIM2_CH1				SPI_MISO	RTC_OUT	ATIM_CH2B
PB15	GTIM2_CH2		BTIM2_TOGN		SPI_MOSI	RTC_1Hz	ATIM_CH3B

Table 5-5 Alternate functions selected through GPIOC_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC13	UART1_TXD	RTC_1Hz	UART1_CTS	RTC_OUT	BTIM_ETR		RTC_TAMP
PC14	AWT_ETR	UART2_TXD	UART1_RTS	BTIM2_TOGN	UART2_RXD		
PC15	HSE_OUT	UART2_RXD	MCO_OUT	BTIM2_TOGP	UART2_TXD	UART1_RXD	

Table 5-6 Alternate functions selected through GPIOF_AFRy registers

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF00	AWT_ETR	UART3_TXD	I2C_SDA	BTIM1_TOGN	UART3_RXD	GTIM2_TOGP	
PF01	LSE_OUT	UART3_RXD	I2C_SCL	BTIM1_TOGP	UART3_TXD	GTIM2_TOGN	
PF06	UART3_CTS	I2C_SCL		UART2_CTS			BTIM3_TOGN
PF07	UART3_RTS	I2C_SDA		UART2_RTS			BTIM3_TOGP

6 Address mapping

The CW32W031 kernel has a maximum address space of 4GB. The built-in program memory, data memory, peripherals and port registers are addressed in the same 4GB linear address space. The RF subsystem has a separate physical address space and the M0+ core accesses the RF subsystem through the internal high-speed SPI interface.

Figure 6-1 CW32W031 internal address mapping

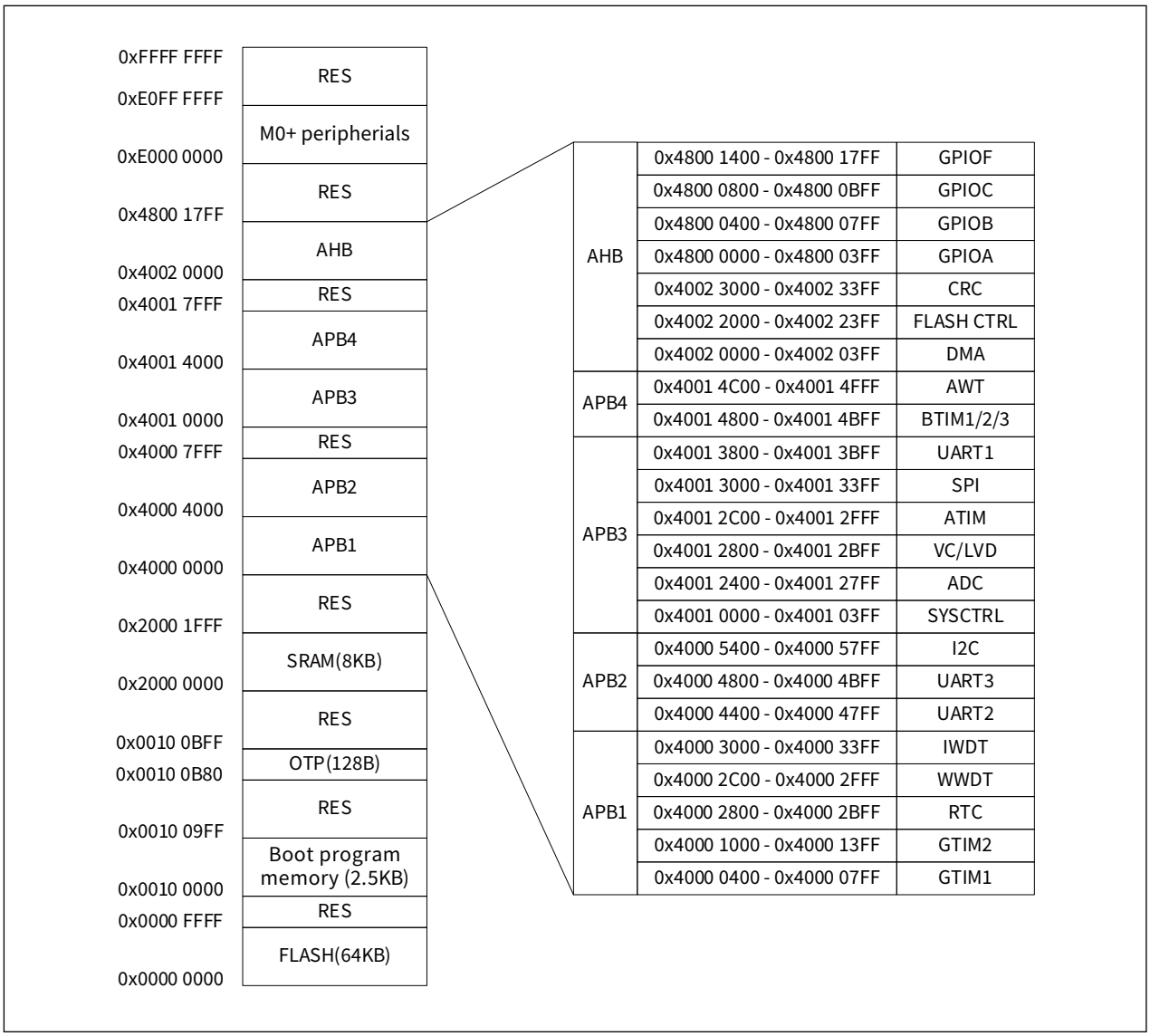


Table 6-1 CW32W031 peripheral register boundary addresses

Device or bus	Boundary address	Size	Peripheral
Main FLASH memory	0x0000 0000 - 0x0000 FFFF	64KB	Main FLASH
OTP memory	0x0010 0B80 - 0x0010 0BFF	128B	OTP
Boot program memory	0x0010 0000 - 0x0010 09FF	2.5KB	BootLoader
SRAM memory	0x2000 0000 - 0x2000 1FFF	8KB	SRAM
APB1 peripheral	0x4000 0400 - 0x4000 07FF	1KB	GTIM1
	0x4000 1000 - 0x4000 13FF	1KB	GTIM2
	0x4000 2800 - 0x4000 2BFF	1KB	RTC
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDT
	0x4000 3000 - 0x4000 33FF	1KB	IWDT
APB2 peripheral	0x4000 4400 - 0x4000 47FF	1KB	UART2
	0x4000 4800 - 0x4000 4BFF	1KB	UART3
	0x4000 5400 - 0x4000 57FF	1KB	I2C
APB3 peripheral	0x4001 0000 - 0x4001 03FF	1KB	SYSCTRL
	0x4001 2400 - 0x4001 27FF	1KB	ADC
	0x4001 2800 - 0x4001 2BFF	1KB	VC/LVD
	0x4001 2C00 - 0x4001 2FFF	1KB	ATIM
	0x4001 3000 - 0x4001 33FF	1KB	SPI
	0x4001 3800 - 0x4001 3BFF	1KB	UART1
APB4 peripheral	0x4001 4800 - 0x4001 4BFF	1KB	BTIM1/2/3
	0x4001 4C00 - 0x4001 4FFF	1KB	AWT
AHB peripheral	0x4002 0000 - 0x4002 03FF	1KB	DMA
	0x4002 2000 - 0x4002 23FF	1KB	FLASH CTRL
	0x4002 3000 - 0x4002 33FF	1KB	CRC
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
M0+ peripheral	0xE000 0000 - 0xE00F FFFF	1MB	M0+ peripheral

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3Σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C and V_{DD} = 3.3V. They are given only as design guidelines and are not tested.

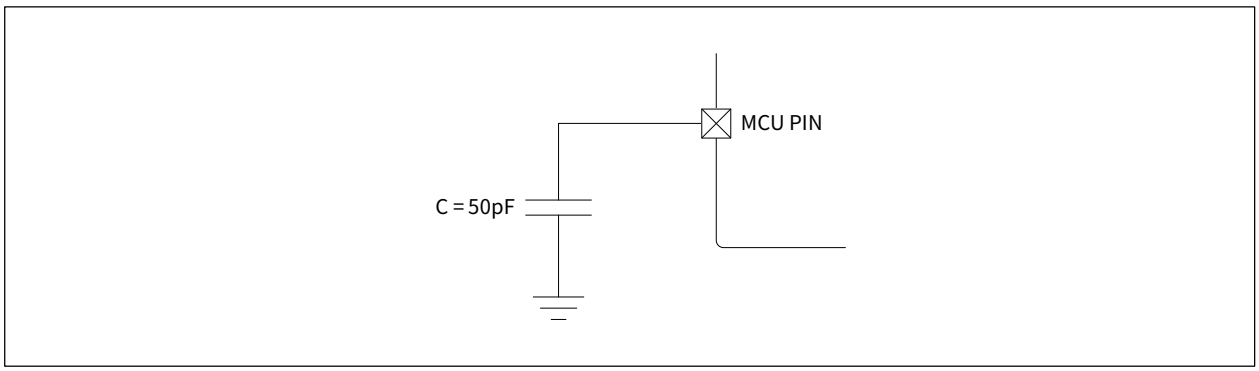
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below:

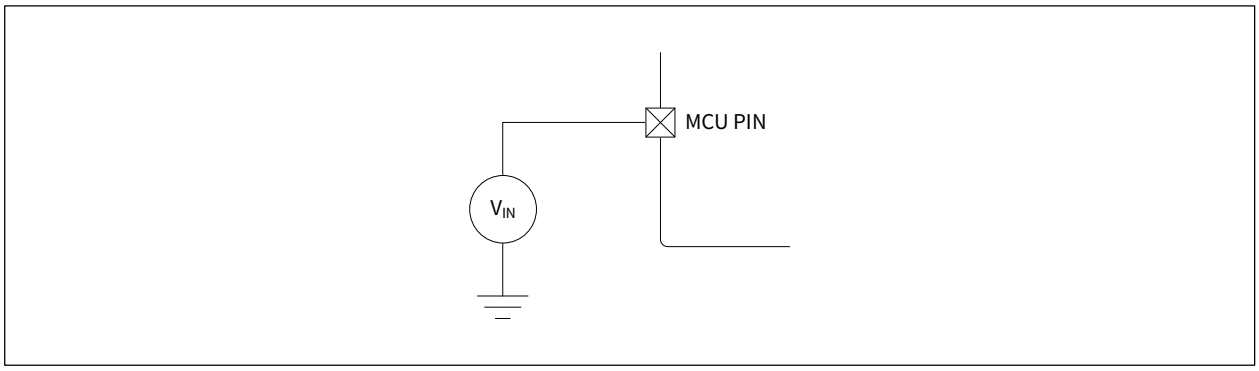
Figure 7-1 Pin loading conditions



7.1.5 Pin input voltage

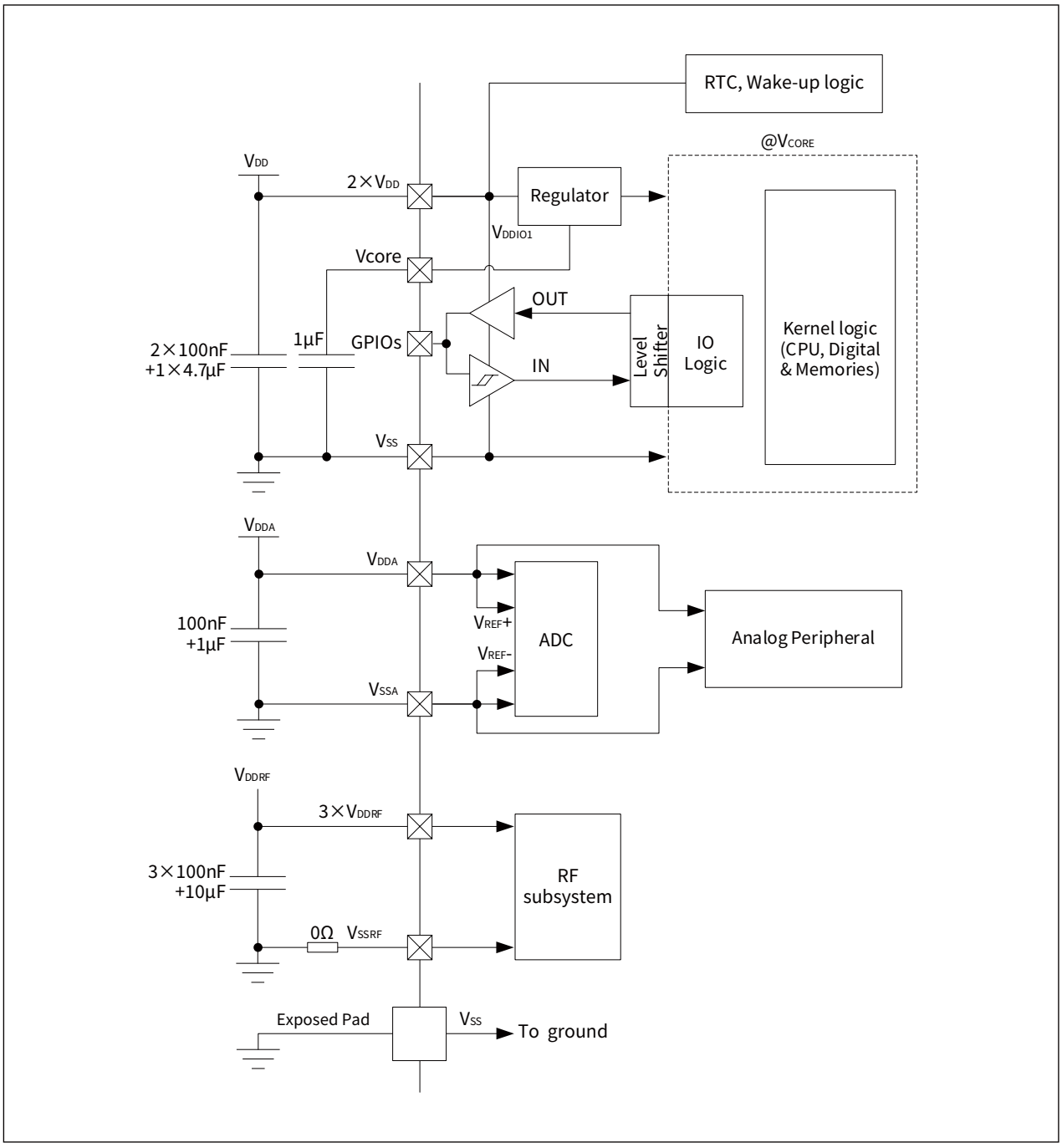
The input voltage measurement on a pin of the device is described in the figure below:

Figure 7-2 Pin input voltage



7.1.6 Power system

Figure 7-3 Power system



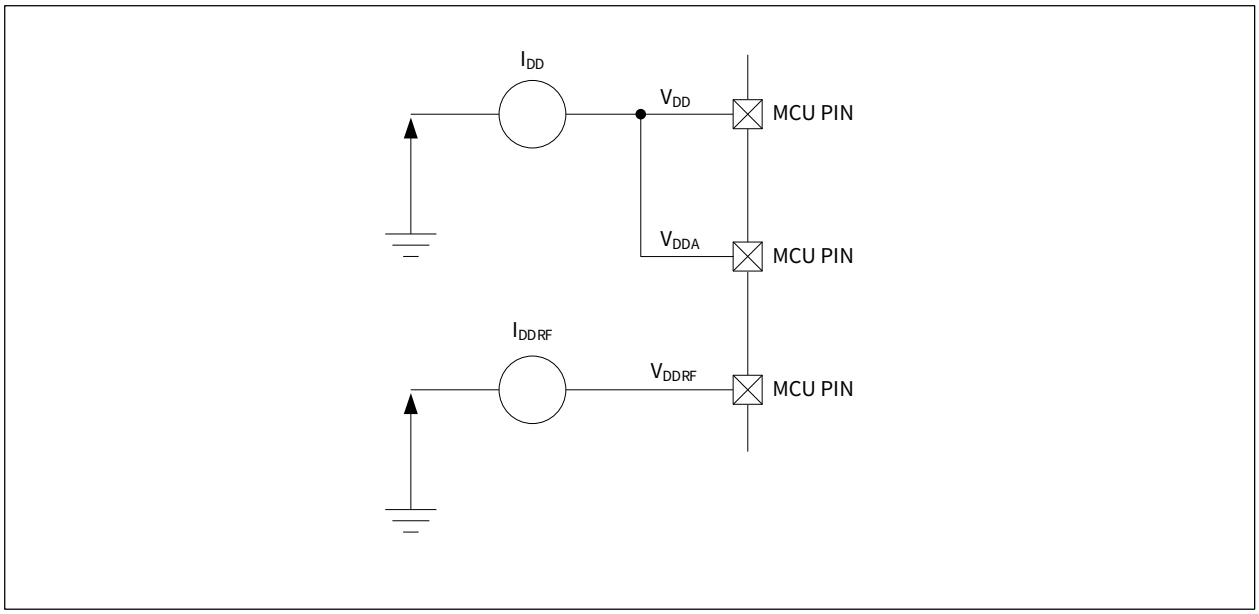
Caution 1: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA}, V_{DDRF}/V_{SSRF} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Caution 2: All V_{DD} pins must be powered and at the same voltage.

Caution 3: Vcore is the regulator supply output and must be connected to a 1μF capacitor to ground and is for internal circuit use only.

7.1.7 Current consumption measurement

Figure 7-4 Method of measurement



7.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 7-1, Table 7-2 and Table 7-3 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7-1 Voltage characteristics[1]

Symbol	Ratings	Min.	Max.	Unit
V_{DD} - V_{SS}	External main supply voltage	-0.3	3.6	V
V_{DDA}-V_{SS}	External analog supply voltage	-0.3	3.6	V
V_{DDRF}-V_{SS}	External RF supply voltage	-0.3	3.6	V
V_{DD}-V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.3	V
V_{IN}[2]	Input voltage on port IO	V_{SS} - 0.3	V_{DD}	V
$\lvert \Delta V_{DDx} \rvert$	Variations between all the different V_{DD} pins	-	0.05	V
$\lvert V_{SSX}$-$V_{SS} \rvert$	Variations between all the different V_{SS} pins	-	0.05	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	*See Table 7-24 ESD characteristics*		kV

Caution 1: All main power (V_{DD}, V_{DDA}, V_{DDRF}) and ground (V_{SS}, V_{SSA}, , V_{SSRF}) pins must always be connected to the external power supply, in the permitted range.

Caution 2: V_{IN} maximum must always be respected，refer to Table 7-2 for the maximum allowable injection current value.

Table 7-2 Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source) [1]	+120	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} power lines (sink) [1]	-120	
$I_{VDD(PIN)}$	Total current into sum of a single V_{DD} power lines (source) [1]	+100	
$I_{VSS(PIN)}$	Total current out of sum of a single V_{SS} power lines (sink) [1]	-100	
$I_{IO(PIN)}$	Current into a single I/O or control pin	+25	
	Current out of a single I/O or control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os or control pins	+80	
	Total output current sourced by sum of all I/Os or control pins	-80	
$I_{INJ(PIN)}$ [2、3]	Injected current on TC and RST pins	±5	
	Injected current on TTa pins	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) [4]	±25	

Caution 1: All main power (V_{DD}, V_{DDA}, V_{DDRF}) and ground (V_{SS}, V_{SSA}, , V_{SSRF}) pins must always be connected to the external power supply, in the permitted range.

Caution 2: $I_{INJ(PIN)}$ must not exceed its limit to ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed to not to exceed its maximum value, also ensure that external limit $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.

Caution 3: Negative injection disturbs the analog performance of the device.

Caution 4: When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents. This result is based on the characterization of the maximum value of $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-55 to +125	°C
T_J	Maximum junction temperature	105	

7.3 Operating conditions

7.3.1 General operating conditions

Table 7-4 General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB bus frequency	-	0	48	MHz
f_{PCLK}	Internal APB bus frequency	-	0	48	
V_{IN}	I/O input voltage	TC I/O	-0.3	V_{DD} + 0.3	V
		TTa I/O	-0.3	V_{DDA} + 0.3	
		BOOT	-0.3	V_{DD}+0.3	
RF LDO mode					
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}	Analog operating voltage	Must be equal to V_{DD}	1.8	3.6	
V_{DDRF}	RF operating voltage	-	1.8	3.6	
RF DCDC mode					
V_{DD}	Standard operating voltage	-	2.0	3.6	V
V_{DDA}	Analog operating voltage	Must be equal to V_{DD}	2.0	3.6	
V_{DDRF}	RF operating voltage	-	2.0	3.6	

7.3.2 RF ChirpIoT ™ characteristics

The RF is in the following test conditions:

- T_A = 25°C , V_{DDRF} = 3.3V
- Frequency: 490MHz
- Error correcting code = 4/8
- Packet error rate ⩽ 5%
- Payload length = 10Bytes
- LDO mode

Table 7-5 RF ChirpIoT ™ characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{OP}	Operating frequency	-	370	-	590	MHz
		-	740	-	1180	
F_{XTAL}	Crystal frequency	-	-	32	-	
R_S	Crystal series resistance	-	-	30	50	Ω
C_{FOOT}	Crystal external capacitance	-	8	15	22	pF
C_{LOAD}	Crystal load capacitance	-	6	10	12	
F_{TOL}	Initial frequency tolerance	-	-	±10	-	ppm
BR	Bit rate	-	0.08	-	20.4	kbps

Caution 1: Channels up to an integer multiple of 8 and up to an integer multiple of 8 ± 400 kHz are not recommended.

Caution 2: The inter-channel spacing needs to be greater than 2 x BW (bandwidth) and cannot be a multiple of 1MHz ~ 1.1MHz.

Caution 3: When operating in the 863MHz ~ 870MHz and 902MHz ~ 928MHz bands, it is recommended that the value of address 0x63 in the RF register Page1 be configured as 0xE7 if the ETSI specification is to be exceeded and the maximum power level cannot be used.

Table 7-6 RF transmitting characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
P_{LPWAN}	Output power	-	-7	-	22	dBm

Caution 1: The data is based on the 490MHz frequency point, other frequency bands may differ in their specifications

Table 7-7 RF receiving characteristic

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RF_62.5	RF sensitivity, long range mode, highest LNA gain, 62.5kHz bandwidth using separate RX/TX channels	SF=7	-	-126	-	dBm
		SF=10	-	-135	-	
		SF=12	-	-140	-	
RF_125	RF sensitivity, long range mode, highest LNA gain, 125kHz bandwidth using separate RX/TX channels	SF=7	-	-124	-	
		SF=10	-	-132	-	
		SF=12	-	-137	-	
RF_250	RF sensitivity, long range mode, highest LNA gain, 250kHz bandwidth using separate RX/TX channels	SF=7	-	-121	-	
		SF=10	-	-129	-	
		SF=12	-	-134	-	
RF_500	RF sensitivity, long range mode, highest LNA gain, 500kHz bandwidth using separate RX/TX channels	SF=7	-	-119	-	
		SF=10	-	-126	-	
		SF=12	-	-132	-	

Caution 1: The data is based on the 490MHz frequency point, other frequency bands may differ in their specifications

Caution 2: The DCDC mode is 1dB ~ 3dB less sensitive than the LDO mode.

Table 7-8 RF current consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DDRF}	RF current consumption	DeepSleep mode	-	400	-	nA
		TX mode @ 0dBm output power	-	25	-	mA
		TX mode @ 18dBm output power	-	83	-	
		TX mode @ 22dBm output power	-	135	-	
		RX mode @DCDC mode, max LNA gain	-	12.5	-	
		RX mode @LDO mode, max LNA gain	-	18	-	

Table 7-9 RF I/O characteristic

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high level voltage	-	V_{DDRF}-0.3	-	V_{DDRF}	V
V_{OL}	Output low level voltage	-	V_{SSRF}	-	V_{SSRF}+0.3	
V_{IH}	Input high level voltage	-	0.8×V_{DDRF}	-	-	
V_{IL}	Input low level voltage	-	-	-	0.2×V_{DDRF}	
f_{SCK}	SPI clock frequency	-	-	-	10	Mbps

7.3.3 Operating conditions at power-up/power-down

The parameters given in the table below are tested under the working conditions listed in *Table 7-4 General operating conditions*.

Table 7-10 Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	μs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

7.3.4 Embedded reset and power control block characteristics

The parameters given in the table below are tested under the working conditions listed in *Table 7-4 General operating conditions*.

Table 7-11 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{POR/BOR}$	Power on/power down reset threshold	Falling edge	1.45 [1]	1.50	1.55 [2]	V
		Rising edge	1.50 [2]	1.55	1.60	V
$V_{BORhyst}$ [3]	BOR hysteresis	-	-	50	-	mV
$t_{RSTTEMPO}$ [3]	Reset temporization	-	4	6.5	13	ms

Caution 1: The product behavior is guaranteed by design down to the minimum $V_{POR/BOR}$ value.

Caution 2: Data based on characterization results, not tested in production.

Caution 3: Guaranteed by design, not tested in production.

7.3.5 Internal reference voltage

Table 7-12 Internal reference voltage

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{REFINT1V5}$	Internal 1.5V reference voltage	-40°C < T_A < +85°C	1.485	1.50	1.515	V
$V_{REFINT2V5}$	Internal 2.5V reference voltage	-40°C < T_A < +85°C	2.475	2.50	2.525	V
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3V	-	-	10 [1]	mV
T_{Coeff}	Temperature coefficient	-	-60 [1]	-	+60 [1]	ppm/°C

Caution 1: Guaranteed by design, not tested in production.

7.3.6 Supply current characteristics

Current consumption is affected by many factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

Figure 7-4 Method of measurement shows the circuit for testing current consumption.

All result of the Run-mode current consumption measurements based on the same limited code used to test CoreMark.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to thef_{HCLK} frequency :
  - 0 wait state inserted when 0 to 24MHz
  - 1 wait state inserted when above 24MHz
  - 2 wait state inserted when above 48MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The data given in Table 7-8 to Table 7-11 are derived from tests performed under the ambient temperature and supply voltage noted in the remarks. For the test conditions, please refer to *Table 7-4 General operating conditions*。

Table 7-13 Typical and maximum current consumption at $V_{DD} = V_{DDA} = 3.6V$

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled		All peripherals disabled		Unit
				Typ.	Max.[1] $T_A = 85°C$	Typ.	Max.[1] $T_A = 85°C$	
I_{DD}[2]	Supply current in Active mode, (code executing from Flash)	HSI or HSE clock	48MHz	7.2	8.2	4.6	5.2	mA
			24MHz	5.0	5.7	3.7	4.2	
I_{DD}	Supply current in Active mode (code executing from RAM)	HSI or HSE clock	48MHz	5.3	5.9	2.6	2.9	mA
			24MHz	2.9	3.2	1.5	1.7	
I_{DD}	Supply current in Sleep mode (code executing from Flash or RAM)	HSI or HSE clock	48MHz	3.8	4.2	1.1	1.23	mA
			24MHz	2.1	2.4	0.75	0.86	

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.
Caution 2: I_{DD} is the total current consumption of V_{DD} and V_{DDA}.

Table 7-14 Current consumption when system clock is LSE

Symbol	Parameter	Conditions		V_{DD} = 1.8V~3.6V		V_{DD} = 3.3V	Unit
				Min.[1]	Max.[1]	Typ.	
I_{DD}[2]	Supply current in Active mode (code executing from FLASH, all peripheral clocks enabled)	LSE=32768Hz (AMP=0，DRIVER=0)	T_A= -40°C	7.6	8.7	8.1	µA
			T_A= 25°C	8.0	8.7	8.2	
			T_A= 50°C	8.6	9.3	8.8	
			T_A= 85°C	12.0	13.4	12.7	
	Supply current in Active mode (code executing from FLASH, all peripheral clocks disabled)	LSE=32768Hz (AMP=0，DRIVER=0)	T_A= -40°C	5.8	6.9	6.3	
			T_A= 25°C	6.2	6.9	6.4	
			T_A= 50°C	6.8	7.5	7.0	
			T_A= 85°C	10.3	11.6	10.9	

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.
Caution 2: I_{DD} is the total current consumption of V_{DD} and V_{DDA}.

Table 7-15 Typical and maximum current consumption in DeepSleep

Symbol	Parameter	Conditions	Typ. @V_{DD} (V_{DD} = V_{DDA})	Max.[1]	Unit
			3.6V	T_A=85°C	
I_{DD}[2]	Supply current in DeepSleep mode	The regulator is in Active mode, all oscillators are off	0.45	3.84	µA
		The regulator is in Active mode, LSI and IWDT are on	1.11	4.65	

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.
Caution 2: I_{DD} is the total current consumption of V_{DD} and V_{DDA}.

Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3V$
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency:
  - 0 wait state inserted when 0 to 24MHz
  - 1 wait state inserted when above 24MHz
  - 2 wait state inserted when above 48MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Table 7-16 Typical current consumption in Active mode, program running from FLASH

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD} [1]	Supply current in Active mode	Runs from FLASH with 8MHz external crystal oscillator clock	48MHz	7.2	4.6	mA
			8MHz	2.1	1.6	

Caution 1: I_{DD} is the total current consumption of V_{DD} and V_{DDA}.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

- I/O static current consumption

  All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up resistors values given in *Table 7-25 I/O static characteristics*.

  For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

  If the input voltage level of the I/Os is the intermediate voltage level, it will continuously cause the internal Schmitt trigger to flip, resulting in additional random current consumption (although it is small). If it is required to judge the level flip situation in real time, that should configure the I/Os in analog input mode to avoid this.

Caution 1: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

- I/O dynamic current consumption

  In addition to the internal peripheral current consumption measured previously, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

  where:

  I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load.

  V_{DDIOx} is the I/O supply voltage.

  f_{SW} is the I/O switching frequency.

  C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

  C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 7-17 Switching output I/O current consumption

Symbol	Parameter	Conditions [1]	I/O toggling frequency (f_{SW})	Typ.	Unit
I_{SW}	I/O current consumption	V_{DDIOx} = 3.3V C_{EXT} = 0pF $C = C_{INT} + C_{EXT} + C_S$	4MHz	0.18	mA
			8MHz	0.37	
			16MHz	0.76	
			24MHz	1.39	
		V_{DDIOx} = 3.3V C_{EXT} = 22pF $C = C_{INT} + C_{EXT} + C_S$	4MHz	0.49	
			8MHz	0.94	
			16MHz	2.38	
			24MHz	3.99	
		V_{DDIOx} = 3.3V C_{EXT}= 47pF $C = C_{INT} + C_{EXT} + C_S$	4MHz	0.81	
			8MHz	1.7	
			16MHz	3.67	

Caution 1: C_S = 7pF (estimated value).

7.3.7 Wakeup time from low-power mode

The wakeup times given in the table below are tested during the wake-up phase of the HSIOSC.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode and DeepSleep mode.

All test environments are from ambient temperature and supply voltage conditions summarized in *Table 7-4 General operating conditions*.

Table 7-18 Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ. @V_{DD} (V_{DD} = V_{DDA})	Max.	Unit
			3.3V		
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4	4	HCLK
t_{WUDEEP}	Wakeup form DeepSleep mode	Regulator in Active mode	4.0	5.0	µs

7.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

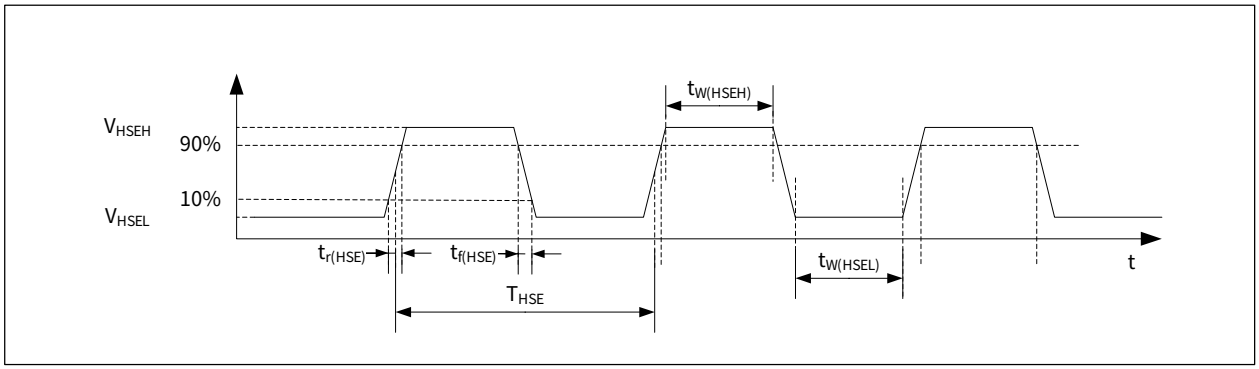
The external clock signal has to respect the I/O characteristics in Section *7.3.11 I/O port characteristics.* The recommended clock input waveform is shown in *Figure 7-5 High-speed external clock source AC timing diagram*.

Table 7-19 High-speed external clock input characteristics

Symbol	Parameter [1]	Min.	Typ.	Max.	Unit
f_{HSE_EXT}	User external clock source frequency	1	-	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

Caution 1: Guaranteed by design, not tested in production.

Figure 7-5 High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

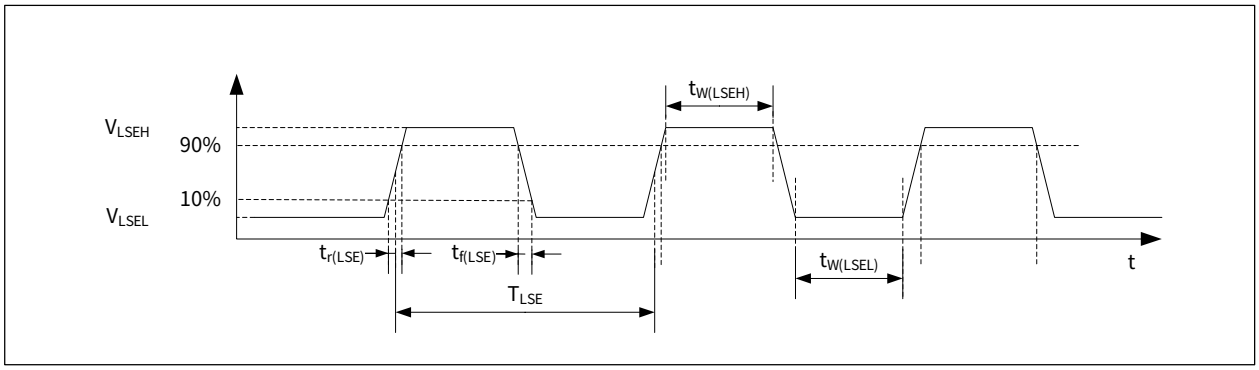
The external clock signal has to respect the I/O characteristics in Section *7.3.11 I/O port characteristics.* The recommended clock input waveform is shown in *Figure 7-6 Low-speed external clock source AC timing diagram*.

Table 7-20 Low-speed external clock input characteristics

Symbol	Parameter [1]	Min.	Typ.	Max.	Unit
f_{LSE_EXT}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{W(LSEH)}$ $t_{W(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

Caution 1: Guaranteed by design, not tested in production.

Figure 7-6 Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 7-21 HSE oscillator characteristics

Symbol	Parameter	Conditions [1]	Min. [2]	Typ.	Max. [2]	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	1.4	-	MΩ
I_{DD}	HSE current consumption	During startup [3]	-	-	900	μA
		V_{DD}= 3.3 V, R_m = 45 Ω, C_L = 10 pF@8 MHz	-	430	-	
		V_{DD} = 3.3 V, R_m = 30 Ω, C_L = 20 pF@32 MHz	-	980	-	
$t_{su(HSE)}$ [4]	Startup time	V_{DD} is stabilized	-	2	-	ms

Caution 1: Resonator characteristics given by the crystal/ceramic resonator manufacturer.

Caution 2: Guaranteed by design, not tested in production.

Caution 3: This consumption level occurs during the first 2/3 of the $t_{su(HSE)}$ startup time.

Caution 4: $t_{su(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 7-22 LSE oscillator characteristics (f_{LSE} = 32.768kHz)

Symbol	Parameter [1]	Conditions	Min. [1]	Typ.	Max. [1]	Unit
I_{DD}	LSE current consumption	low drive capability	-	0.35	0.45	μA
		medium-low drive capability	-	0.45	0.60	
		medium-high drive capability	-	0.70	0.90	
		high drive capability	-	1.60	2.00	
$t_{su(LSE)}$ [2]	Startup time	V_{DD} stabilized	-	1.50	-	s

Caution 1: Guaranteed by design, not tested in production.

Caution 2: $t_{su(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

7.3.9 Internal clock source characteristics

The data given in the following table is based on the sample tests of the test environment indicated by *Table 7-4 General operating conditions*.

High-speed internal (HSIOSC) RC oscillator

Table 7-23 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
TRIM	HSI user trimming step	-	-	0.2	-	%
$Duty_{HSI}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = -40°C ~ +85°C	-2.0	-	+2.0	%
		T_A = +25°C	-0.5	-	+0.5	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	3	-	5	μs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	600	-	μA

Low-speed internal (LSI) RC oscillator

Table 7-24 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	-	32.8	-	kHz
TRIM	LSI user trimming step	-	-	1	-	%
$Duty_{LSI}$	Duty cycle	-	45	-	55	%
ACC_{LSI}	Accuracy of the LSI oscillator (factory calibrated)	T_A = -40°C ~ +85°C	-3	-	+3	%
		T_A = +25°C	-1	-	+1	%
$t_{SU(LSI)}$	LSI oscillator startup time	-	-	-	50	μs
$I_{DDA(LSI)}$	LSI oscillator power consumption	-	-	1	-	μA

Ultra-Low-Speed Internal (RC10K) RC Oscillator

Table 7-25 RC10K oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{RC10K}	Frequency	-	-	8	-	kHz
$Duty_{RC10K}$	Duty cycle	-	45	-	55	%
ACC_{RC10K}	Accuracy of the RC10K oscillator(factory calibrated)	T_A = -40°C ~ +85°C	-50	-	+50	%
		T_A = +25°C	-20	-	+20	%

Mid-low-speed internal (RC150K) RC oscillator

Table 7-26 RC150K oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{RC150K}	Frequency	-	-	120	-	kHz
$Duty_{RC150K}$	Duty cycle	-	45	-	55	%
ACC_{RC150K}	Accuracy of the RC150K oscillator(factory calibrated)	T_A = -40°C ~ +85°C	-50	-	+50	%
		T_A = +25°C	-20	-	+20	%

7.3.10 Memory characteristics

FLASH memory

The characteristics are for 40°C to +85°C test enviroment unless otherwise specified.

Table 7-27 FLASH memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max. [1]	Unit
t_{prog8}	8-bit programming time	T_A = -40°C ~ +85°C	-	30	-	μs
t_{prog16}	16-bit programming time	T_A = -40°C ~ +85°C	-	37	-	μs
t_{prog32}	32-bit programming time	T_A = -40°C ~ +85°C	-	51	-	μs
t_{ERASE}	Page erase time	T_A = -40°C ~ +85°C	-	4.6	-	ms
t_{ME}	Mass erase time	T_A = -40°C ~ +85°C	-	35	-	ms
I_{DD}	Supply current	Write mode	-	-	3.5	mA
		Erase mode	-	-	2.0	mA
V_{prog}	Programming voltage	-	1.8	-	3.6	V

Caution 1: Guaranteed by design, not tested in production.

Table 7-28 FLASH memory endurance and data retention

Symbol	Parameter	Conditions	Min. [1]	Unit
N_{NED}	Endurance	T_A = -40°C ~ +85°C	20000	Times
t_{RET}	Data retention	T_A = 25°C	100	Years
		T_A = 85°C	25	

Caution 1: Obtained by comprehensive evaluation, not tested in production.

7.3.11 ESD characteristics

Use specific measurement methods to test the strength of the chip to determine its electrical sensitivity performance.

Table 7-29 ESD characteristics

Symbol	Parameter	Condition	Typ.	Max.	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A115C	-	-	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-A115C	-	-	

7.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-30 I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	0.3 V_{DDIOx}	V
V_{IH}	High level input voltage	TC and TTa I/O	0.7 V_{DDIOx}	-	-	V
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	400 [1]	-	mV
I_{ikg}	Input leakage current	TC and TTa I/O in digital mode $V_{SS} \leqslant V_{IN} \leqslant V_{DDIOx}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DDIOx} \leqslant V_{IN} \leqslant V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \leqslant V_{IN} \leqslant V_{DDA}$	-	-	±0.2	
R_{PU} [2]	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	45	75	220	kΩ
R_{PD} [2]	Weak pull-down equivalent resistor	$V_{IN} = V_{DDIOx}$	16	30	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Caution 1: Data based on design simulation only. Not tested in production.

Caution 2: Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal.

Output driving current

The GPIOs can sink or source up to ±8mA, and sink or source up to ±20mA with a relaxed V_{OH} and V_{OL}.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section *7.2 Absolute maximum ratings*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 7-1 Voltage characteristics*[1]).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 7-1 Voltage characteristics*[1]).

Output voltage levels

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-31 Output voltage characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	High-level output voltage source current	Sourcing 10mA, V_{DD} = 3.3V[1]	3.02	-	V
		Sourcing 20mA, V_{DD} = 3.3V[2]	2.70	-	
V_{OL}	Low-level output voltage sink current	Sinking 10mA, V_{DD} = 3.3V[1]	-	0.23	
		Sinking 20mA, V_{DD} = 3.3V[2]	-	0.45	

Caution 1: The maximum total current I_{OH}(max) and I_{OL}(max) of all output combinations should not exceed 40mA to meet the maximum specified voltage drop.

Caution 2: The maximum total current I_{OH}(max) and I_{OL}(max) of all output combinations should not exceed 100mA to meet the maximum specified voltage drop.

Input/output AC characteristics

The values and definitions of the AC characteristics of the I/Os are given by the following charts respectively.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

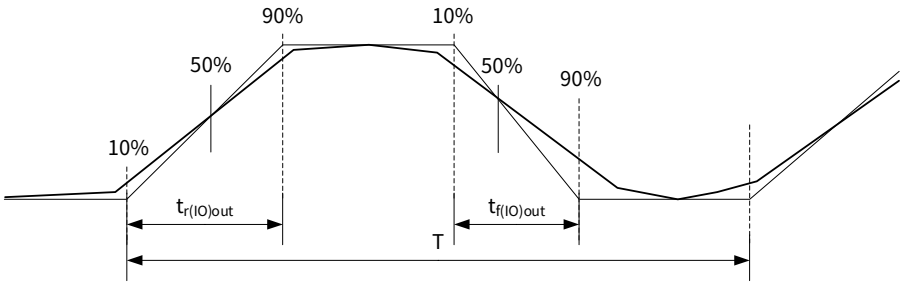
Table 7-32 I/O AC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{max(IO)out}$	Maximum frequency [2]	C_L = 30pF，$V_{DDIOx} \geqslant$ 2.7V	-	50	MHz
		C_L = 50pF，$V_{DDIOx} \geqslant$ 2.7V	-	30	
		C_L = 50pF，2.4V $\leqslant V_{DDIOx} <$ 2.7V	-	20	
$t_{f(IO)out}$	Output fall time	C_L = 30pF，$V_{DDIOx} \geqslant$ 2.7V	-	5	ns
		C_L = 50pF，$V_{DDIOx} \geqslant$ 2.7V	-	8	
		C_L = 50pF，2.4V $\leqslant V_{DDIOx} <$ 2.7V	-	12	
$t_{r(IO)out}$	Output rise time	C_L = 30pF，$V_{DDIOx} \geqslant$ 2.7V	-	5	
		C_L = 50pF，$V_{DDIOx} \geqslant$ 2.7V	-	8	
		C_L = 50pF，2.4V $\leqslant V_{DDIOx} <$ 2.7V	-	12	

Caution 1: Data based on design simulation only. Not tested in production.

Caution 2: The maximum frequency is defined in the figure below.

Figure 7-7 I/O AC characteristics definition



Maximum frequency is achieved if ($t_r + t_f$) $\leqslant$ 2/3T and if the duty cycle is (45-55%) when loaded by C_L

7.3.13 NRST pin characteristics

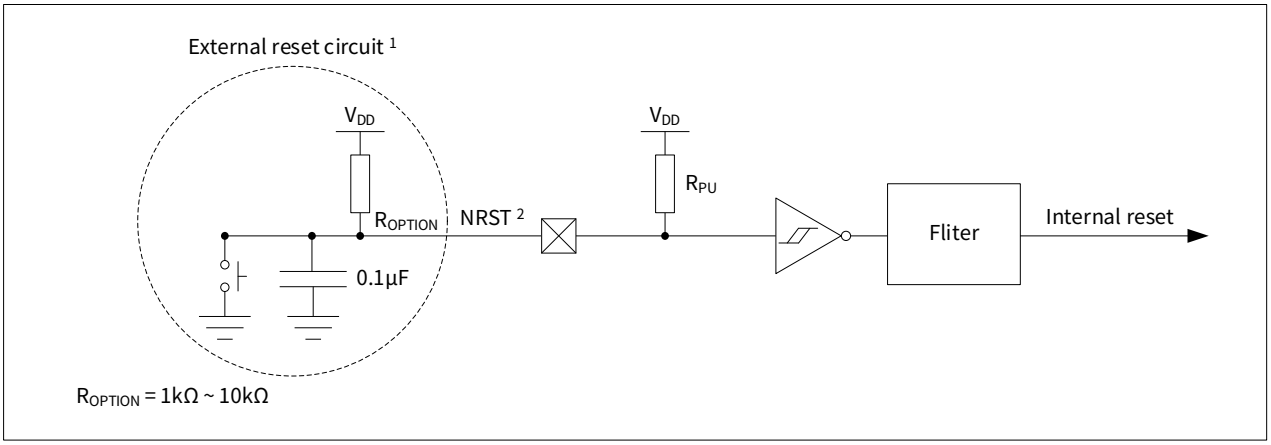
The NRST pin is connected to a permanent pull-up resistor R_{PU} internally.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

Table 7-33 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3V_{DD}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7V_{DD}$	-	-	-
$V_{hys(NRST)}$	NRST input voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	7	8	9	kΩ
$V_{F(NRST)}$	Minimum required reset pulse width	-	20	-	-	μs

Figure 7-8 Recommended NRST pin protection



Caution 1: The external capacitor protects the device against parasitic resets.

Caution 2: The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 7-28 NRST pin characteristics. Otherwise the reset will not be taken into account by the device.

7.3.14 12-bit ADC characteristics

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions.*

Table 7-34 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	1.8	-	3.6	V
$I_{DDA(ADC)}$	Current consumption of the ADC	$V_{DD} = V_{DDA} = 3.3V$	-	1.5	-	mA
f_{ADC}	ADC clock frequency	-	-	24	-	MHz
f_S	Sampling rate	-	-	-	1	MHz
f_{TRIG}	External trigger frequency	$f_{ADC} = 24MHz$	-	-	800	kHz
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}	Input impedance	-	-	-	100	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	9	-	pF
t_S	Sampling time	-	5	-	10	$1 / f_{ADC}$
t_{STAB}	Stabilization time	-	19			$1 / f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	-	24	-	29	$1 / f_{ADC}$

Table 7-35 Accuracy of ADC[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max. [2]	Unit
ET	Composite error	f_{ADC} = 24MHz, V_{DDA} = 1.8V ~ 3.6V, T_A = -40°C ~+85°C	-	±2.5	±3.0	LSB
EO	Offset error		-	±1.5	±2.4	
EG	Gain error		-	±2.2	±2.7	
DNL	Differential nonlinearity		-	±0.5	±1.0	
INL	Integral nonlinearity		-	±1.0	±3.0	
SINAD	Signal-to-noise ratio distortion		-	67	-	dB
SNR	Signal-to-noise ratio		-	66	-	
THD	Total harmonic distortion		-	-70	-	
ENOB	Significant digits	V_{ref} = V_{DDA}/ExRef 100KSPS@V_{DDA} = 1.8V~2V 200KSPS@V_{DDA} = 2V~2.4V	-	10.3	-	bits
		V_{ref} = V_{DDA}/ExRef 500KSPS@V_{DDA} = 2.4V~2.7V 1MSPS@V_{DDA} = 2.7V~3.6V	-	10.8	-	
		V_{ref} = Internal 1.5V reference voltage 100KSPS@V_{DDA} = 1.8V~2V 200KSPS@V_{DDA} = 2V~3.6V	-	9.8	-	
		V_{ref} = Internal 2.5V reference voltage 200KSPS@V_{DDA} = 2.8V~3.6V	-	10.3	-	

Caution 1 : ADC DC accuracy values are measured after internal calibration;

Avoid injecting reverse current on any analogue input pin as this can degrade the accuracy of conversions performed on another analogue input, it is recommended to add a Schottky diode (between the pin and ground) to the analogue pin where the reverse current will probably be injected;

Better performance can be achieved over restricted V_{DDA}, frequency, and temperature ranges.

Caution 2 : Data based on characterization results, not tested in production.

7.3.15 Temperature sensor characteristics

Table 7-36 TS characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L	VSENSE linearity with temperature	-	±2	±5	°C
Avg_Slope	Average slope	2.66	2.69	2.72	mV / °C
V_{25}	Voltage at 25°C（±5°C）	0.77	0.79	0.8	V
t_{START}	TS internal temperature sensor follower settling time	-	-	45	μs
t_{S_temp}	ADC sampling time when reading the temperature	5	-	-	μs

7.3.16 Analog voltage comparator characteristics

Table 7-37 Comparator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max. [1]	Unit
V_{DDA}	Analog supply volgate	-	1.8	-	3.6	V
V_{IN}	Comparator input volgate range	-	0	-	V_{DDA}	V
t_{START}	Startup time	Ultra low speed	-	10	10	μs
		Low speed	-	1	2	
		Medium speed	-	0.5	1	
		High speed	-	0.1	0.25	
t_D	Delay Time	Ultra low speed	-	10	10	
		Low speed	-	1	2	
		Medium speed	-	0.5	1	
		High speed	-	0.2	0.5	
V_{offset}	Offset Error	-	-	±3	±10	mV
dThreshold/dt	Threshold voltage temperature coefficient	V_{DD} = 3.3V, -40°C < T_A < +85°C , V- = (n/64)×V_{ref}	-	40	80	ppm/°C
$I_{DD(VC)}$	Current consumption	Ultra low speed	-	0.2	0.3	μA
		Low speed	-	1	1.2	
		Medium speed	-	8	10	
		High speed	-	16	20	
V_{hys}	Comparator hysteresis	No hysteresis (VCx_CR0.HYS=00)	-	0	-	mV
		Low hysteresis (VCx_CR0.HYS=01)	-	10	-	
		Medium hysteresis (VCx_CR0.HYS=10)	-	20	-	
		High hysteresis (VCx_CR0.HYS=11)	-	30	-	

Caution 1: Data based on characterization results, not production tested.

7.3.17 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to Section *7.3.11 I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 7-38 Timer characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{res(TIM)}$	Timer resolution	-	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 48MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency	-	-	-	f_{TIMCLK} / 2	MHz
t_{MAX_COUNT}	Maximum period	-	-	-	65536	t_{TIMCLK}

Table 7-39 IWDT min/max timeout period at 10 kHz (RC10K)

Frequency division factor	IWDT_CR.PRS	Min timeout period	Max timeout period	Unit
4	0	0.417	2560	ms
8	1	0.834	5120	
16	2	1.667	10240	
32	3	3.334	20480	
64	4	6.667	40960	
128	5	13.334	81920	
256	6	26.667	163840	
512	7	53.334	327680	

Table 7-40 WWDT min/max timeout period at 48 MHz（PCLK）

Frequency division factor	Control bit	Min timeout period	Max timeout period	Unit
4096	0	0.086	3.413	ms
8192	1	0.171	6.826	
16384	2	0.342	13.653	
32768	3	0.683	27.306	
65536	4	1.366	54.613	
131072	5	2.731	109.226	
262144	6	5.461	218.428	
524288	7	10.923	436.906	

7.3.18 Communication interfaces

I2C interface characteristics

- The I2C interface meets the I2C-bus specification and the user manual:
  - Standard-mode (Sm): with a bit rate up to 100 kbit/s
  - Fast-mode (Fm) : with a bit rate up to 400 kbit/s
  - Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s
- The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).
- The SDA and SCL I/O requirements are met with the following restrictions:
  - The SDA and SCL I/O pins are not "true" open-drain,maximum input voltage limited by specification.

    When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present.

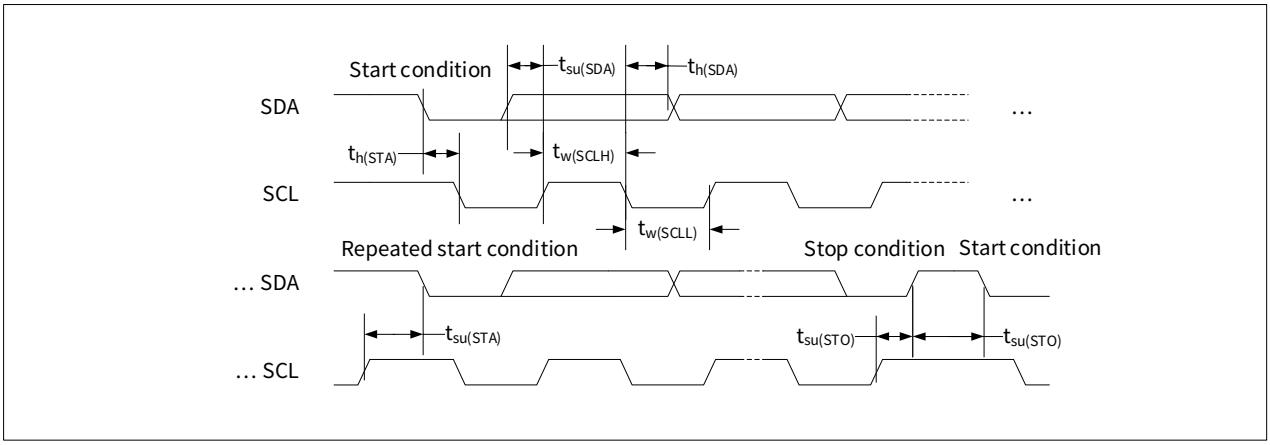
Refer to Section *7.3.11 I/O port characteristics* for the I2C I/Os characteristics.

Table 7-41 I2C characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.25	-	0.5	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	50	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{h(STA)}$	Start condition hold time	2.5	-	0.625	-	0.25	-	µs
$t_{su(STA)}$	Repeated Start Condition Startup Time	2.5	-	0.6	-	0.25	-	
$t_{su(STO)}$	Stop condition setup time	0.25	-	0.25	-	0.25	-	
$t_{w(STO:STA)}$	Stop condition to start condition time(Bus Idle)	4.7	-	1.3	-	0.5	-	

Caution 1: Guaranteed by design, not tested in production.

Figure 7-9 I2C timing diagram



SPI interface characteristic parameters

Table 7-42 SPI characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	10	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C=15pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4\times T_{PCLK}$	-	
$t_{h(NSS)}$	NSS hold time	Slave mode	$2\times T_{PCLK}+10$	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low setup time	Master mode, f_{PCLK}= 48MHz, SCK prescaler divider factor = 4	$T_{PCLK}-2$	$T_{PCLK}+2$	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode (SMP=1)	0	-	
		Slave mode	2	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	2	-	
		Slave mode	2	-	
$t_{v(SO)}$	Data output valid time	Slave mode f_{PCLK}= 48MHz	-	50	
$t_{v(MO)}$		Master mode	-	3	
$t_{h(SO)}$	Data output hold time	Slave mode f_{PCLK}= 48MHz	30	-	
$t_{h(MO)}$		Master mode	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode f_{PCLK}= 48MHz	45	55	%

Caution 1: Data based on characterization results, not tested in production.

Figure 7-10 SPI timing diagram - slave mode and CPHA=0

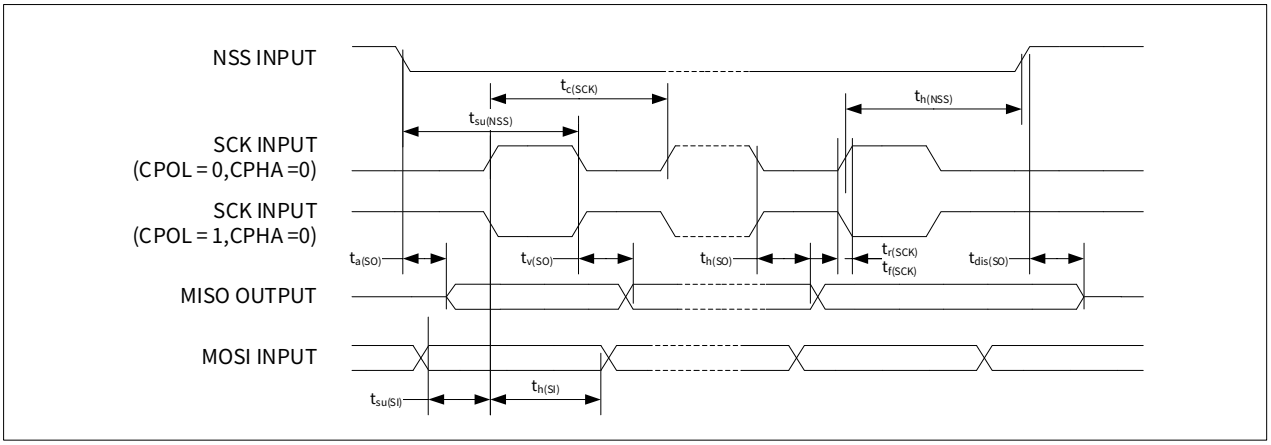


Figure 7-11 SPI timing diagram - slave mode and CPHA=1

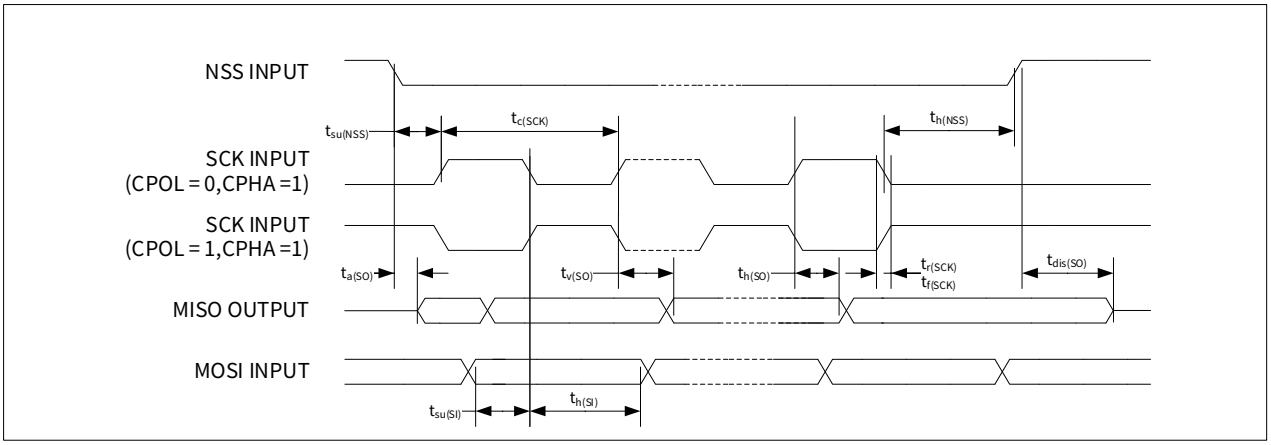
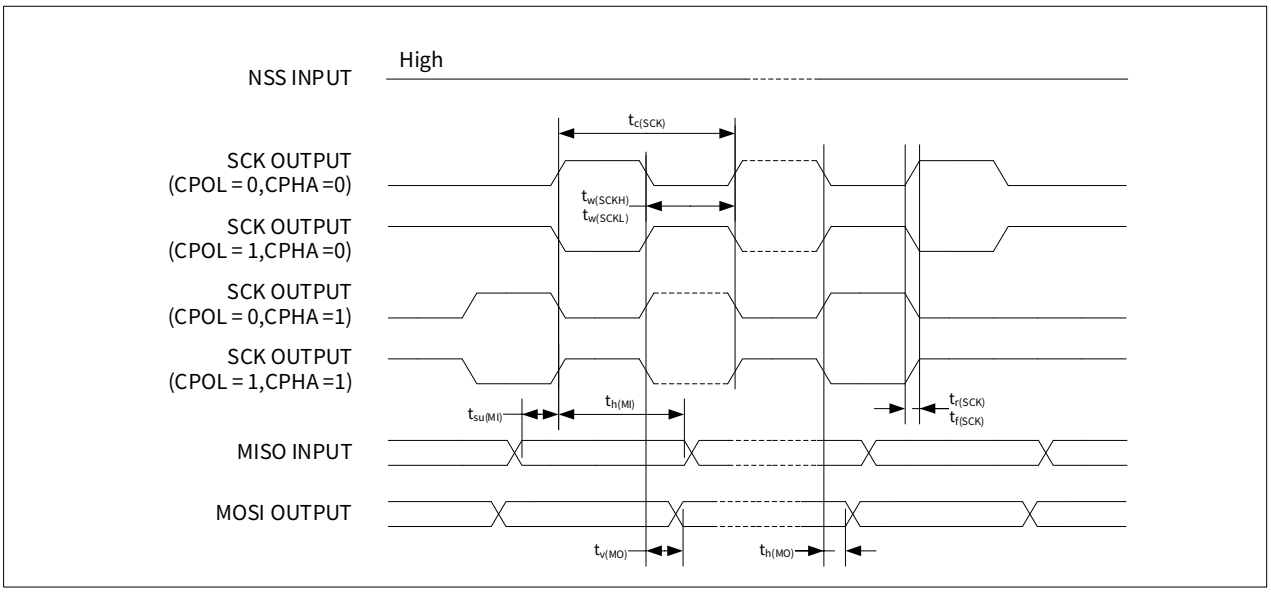


Figure 7-12 SPI timing diagram - master mode

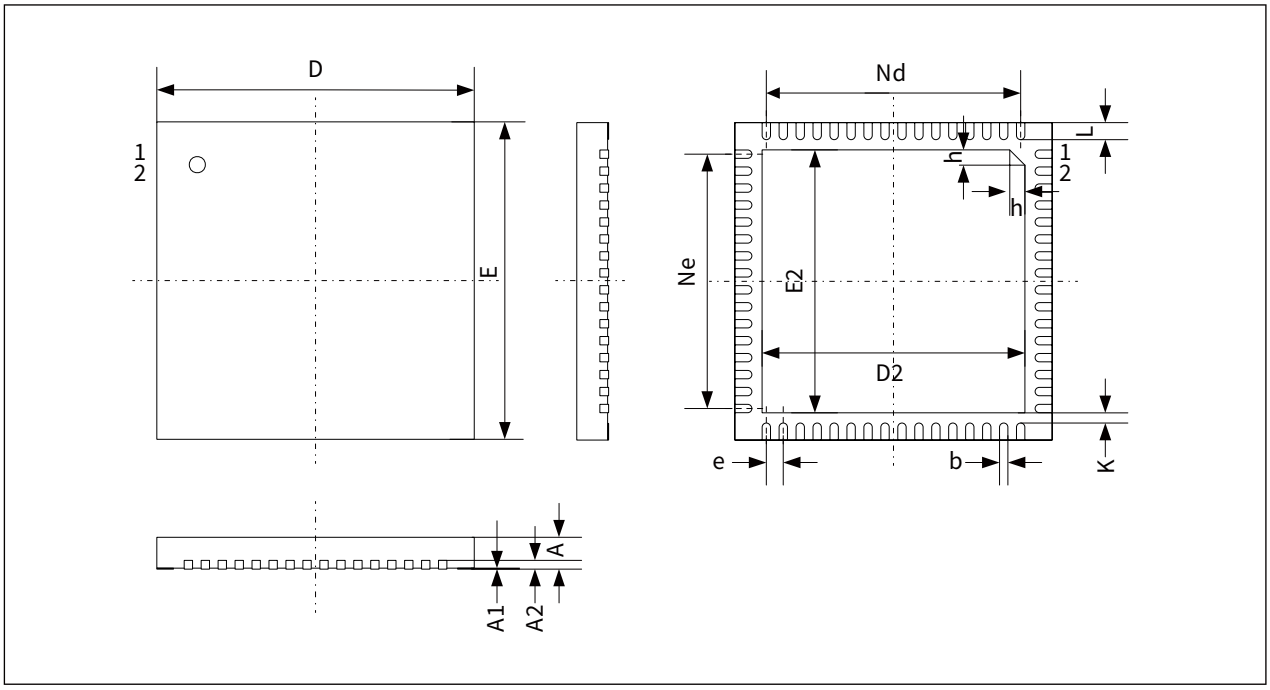


8 Package information

8.1 QFN64 package information

QFN64 is 64-pin, 7.5 x 7.5mm Quad Flat No-leads Package.

Figure 8-1 QFN outline



Caution 1: Drawing is not to scale.

Table 8-1 QFN64 mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.700	0.750	0.800	0.0276	0.0295	0.0315
A1	-	0.020	0.050	-	0.0008	0.0020
A2	0.203 REF			0.0080 REF		
b	0.150	0.200	0.250	0.0059	0.0079	0.0098
D	7.400	7.500	7.600	0.2913	0.2953	0.2992
D2	6.150	6.200	6.250	0.2421	0.2441	0.2461
E	6.900	7.500	7.600	0.2717	0.2953	0.2992
E2	6.150	6.200	6.250	0.2421	0.2441	0.2461
e	0.400 BSC			0.0157 BSC		
K	0.200	0.250	0.300	0.0079	0.0098	0.0118
L	0.350	0.400	0.450	0.0138	0.0157	0.0177
h	0.300	0.350	0.400	0.0118	0.0138	0.0157
Ne	6.000 BSC			0.2362 BSC		
Nd	6.000 BSC			0.2362 BSC		

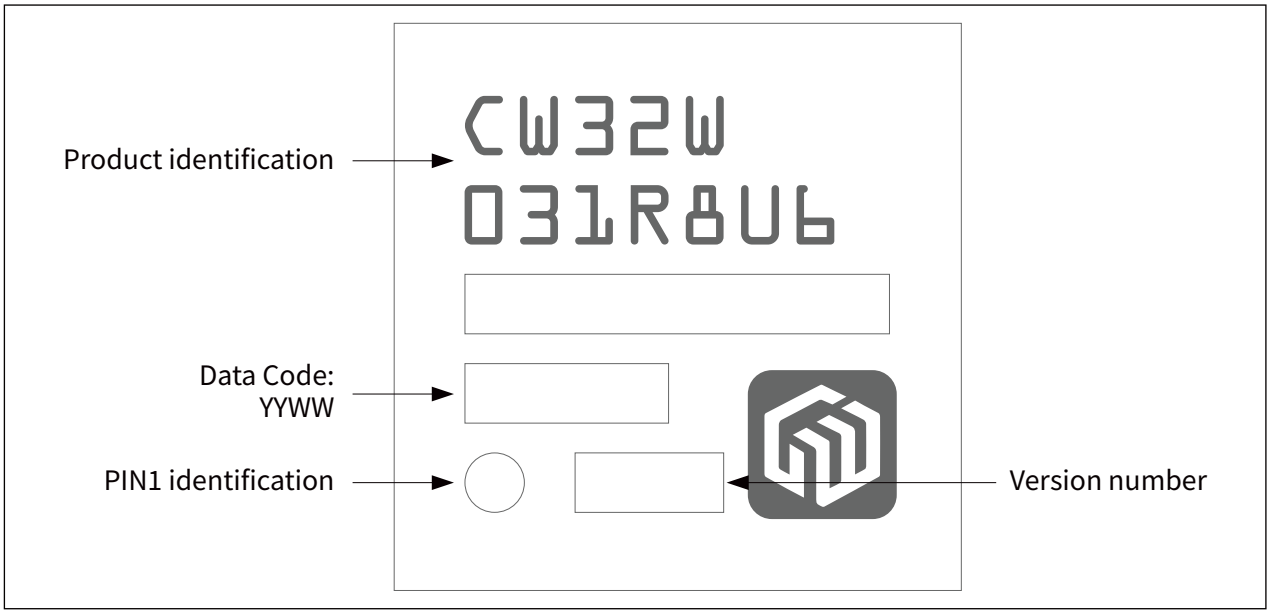
Caution 1: Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-2 QFN64 topside marking example



Caution 1: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

9 Ordering information

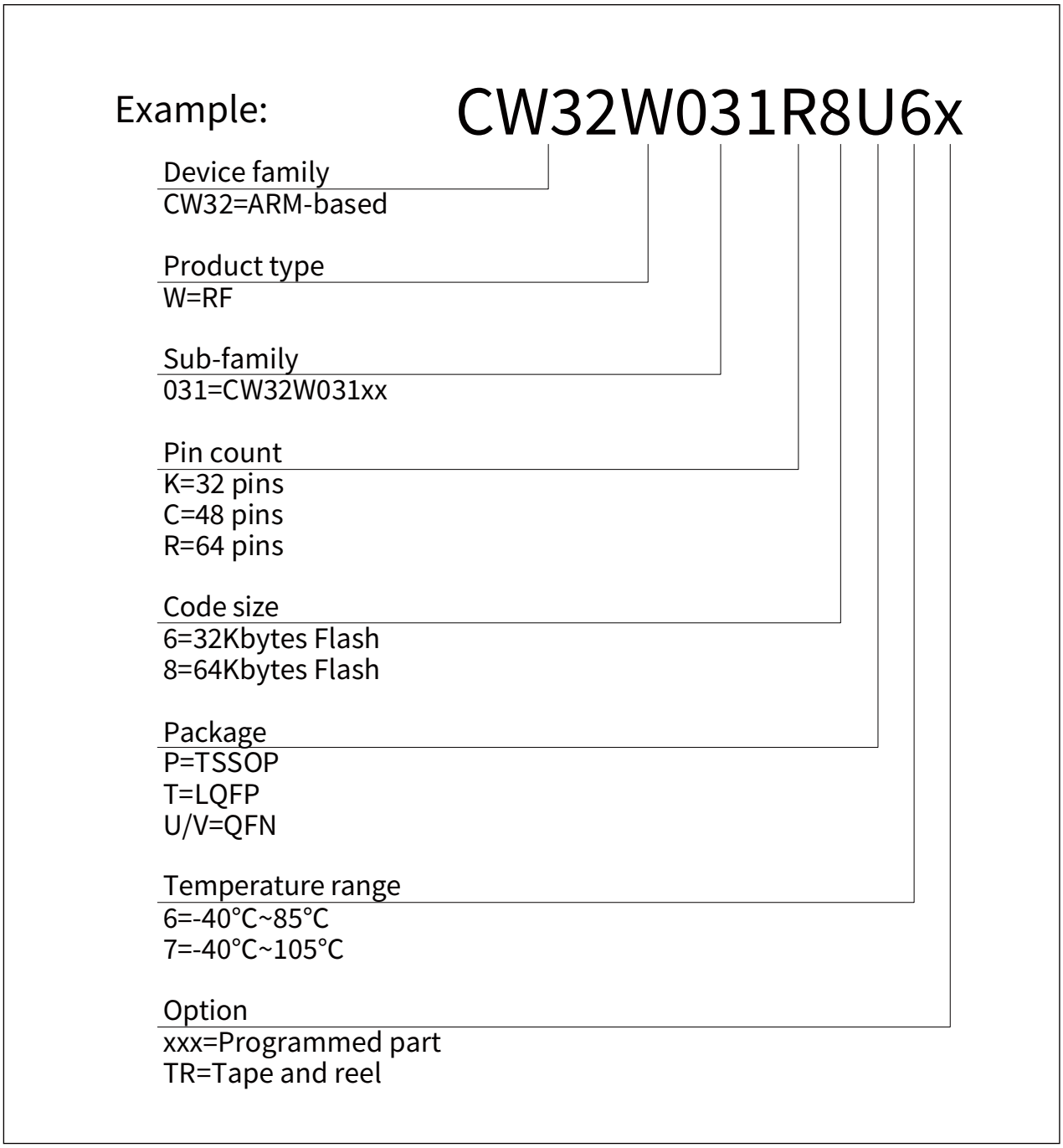


Table 9-1 Minimum Order Quantity (MOQ)

MCU	Packaging	Quantity	MOQ	MSL	Note
CW32W031R8U6	Tray	260 pcs/tray	2600 pcs	3	10 trays/box, 6 boxes/carton, single box vacuumized

10 Revision history

Table 10-1 Document revision history

Date	Revision	Changes
May 18, 2023	Rev 1.0	Initial release.