武汉芯源半导体有限公司
WUHAN XINYUAN SEMICONDUCTOR CO., LTD

CW32F003x3/x4 Datasheet

ARM® Cortex®-M0+ 32-bit MCU with up to 20KB FLASH, 3KB RAM

Rev 1.0

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Contents

1 Features

- Core: ARM® Cortex®-M0+
  - Frequency up to 48MHz
- Operating temperature: -40°C to 105°C ; Operating voltage: 1.65V to 5.5V
- Memories
  - Maximum 20 Kbytes FLASH, data retention 25 years @85°C
  - Up to 3 Kbytes RAM, support parity
  - 22 bytes OTP memory
- CRC calculation unit
- Reset and power management
  - Low power modes (Sleep, DeepSleep)
  - Power-on/Power down reset (POR/BOR)
  - Programmable low voltage detector (LVD)
- Clock management
  - Internal 48MHz RC oscillator
  - Internal 32kHz RC oscillator
  - Internal 10kHz RC oscillator
  - Internal 150kHz RC oscillator
  - External pin input clock
  - Allow independent shutdown of each peripheral clock
- Up to 21 I/O ports
  - All I/Os support interrupt function
  - All I/Os support interrupt input filtering
- Analog to digital converter
  - 12-bit accuracy, ±1 LSB
  - Up to 1M SPS conversion speed
  - Internel voltage reference
  - Analog watchdog function
  - Internal temperature sensor
- Dual voltage comparator

- Timers
  - One 16-bit advanced-control timer for six-channel capture/compare and three pairs of complementary PWM output, dead time ang flexible synchronization function
  - One group of 16-bit general-purpose timers
  - Three groups of 16-bit basic timers
  - Window watchdog timer
  - Independent watchdog timers
- Communication interfaces
  - Two-way low-power UART with fractional baud rate
  - One SPIs (12Mbit/s)
  - One I2Cs (1Mbit/s)
  - IR modulator
- Serial wire debug (SWD)
- 80-bit unique ID

Table 1-1 Package model list

Series	Model	Packages
CW32F003x4	CW32F003E4	TSSOP24
	CW32F003F4	TSSOP20
		QFN20

2 Introduction

This datasheet provides the ordering information and electromechanical characteristics of the CW32F003x3/x4 microcontrollers.

This document should be read in conjunction with the CW32F003 reference manual.

For information on the Arm® Cortex®-M0+ core, please refer to the Cortex®-M0+ Technical Reference Manual, available from the *www.arm.com*.

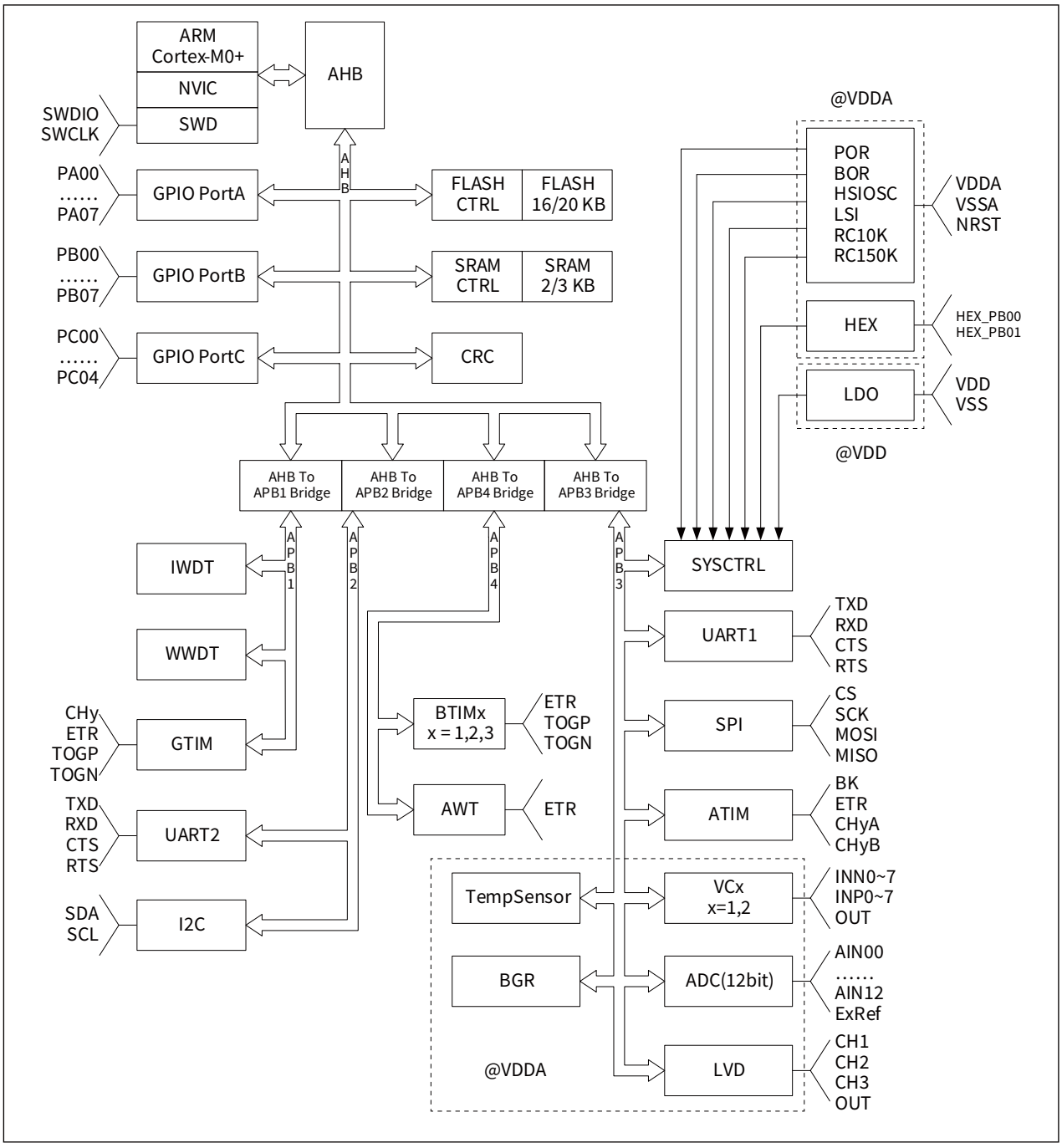
3 Description

CW32F003x3/x4 is an eFlash-based single-chip microcontroller that integrates an ARM® Cortex®-M0+ core with a main frequency up to 48 MHz, high-speed embedded memories(up to 20 Kbytes of FLASH and up to 3 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os.

All devices offer standard communication interfaces (two UARTs, one SPIs, one I2Cs), one 12-bit ADC, four general-purpose and basic timers and an advanced-control PWM timers.

CW32F003x3/x4 operates in the -40 to +105 °C temperature range from a 1.65 to 5.5V power supply. Supports two low-power operating modes, Sleep and DeepSleep. The internal block diagram is shown in the following figure:

Figure 3-1 Internal block diagram



CW32F003x3/x4 provides three different package forms: TSSOP20, QFN20, TSSOP24. The functions that can be realized by products in different packages are different. The details are shown in the following table:

Table 3-1 CW32F003x3/x4 family device features list

Peripheral		CW32F003F4	CW32F003E4
FLASH (Kbytes)		20	20
SRAM (Kbytes)		3	3
Timers	Advanced control	1	1
	General purpose	1	1
	Basic	3	3
SPI		1	1
I2C		1	1
UART		2	2
12 位 ADC (number of channels)		1 (13 ext. + 3 int.)	1 (13 ext. + 3 int.)
GPIO		17	21
Kernel frequency		48MHz	
Operating voltage		1.65V ~ 5.5V	
Operating temperature		-40°C ~ 105°C	
Packages		TSSOP20、QFN20	TSSOP24

4 Functional overview

4.1 ARM® Cortex®-M0+ core with embedded Flash and SRAM

The Arm® Cortex®-M0+ processor is the latest generation 32-bit core for small embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The Arm® Cortex®-M0+ 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the small memory.

The CW32F003 family has an embedded Arm core and is therefore compatible with all Arm tools and software.

4.2 Memories

The device has the following features:

- 2 to 3 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for high reliability critical applications.
- The non-volatile memory is divided into two arrays:
  - 16 to 20 Kbytes of embedded Flash memory for programs and data
  - 2.5 Kbytes of boot program memory
- FLASH memory erasing and reading protection: The FLASH memory erasing and writing protection is performed through the register, and the 4-level read protection level is set through the ISP command.
  - LEVEL0

    No readout protection, the FLASH memory can be read by SWD or ISP.
  - LEVEL1

    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP or SWD interface. After the downgrade, the FLASH is in the whole chip erasing state.
  - LEVEL2

    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. The protection level can be reduced to LEVEL0 through the ISP interface. After the downgrade, the FLASH is in the whole chip erasing state.
  - LEVEL3

    FLASH readout protection, the FLASH memory cannot be read by SWD or ISP. Protection level downgrade in any way is not supported.

4.3 Boot modes

CW32F003 supports the following two boot options:

- Run the internal bootloader
- Run user program

When running the Bootloader, the user can use the ISP communication protocol for FALSH programming through UART1 (pins are PA02/PA05).

4.4 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit can generate the CRC code of the data stream according to the selected algorithm and parameter configuration.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

The product supports four commonly used CRC algorithms, including:

CRC16_CCITT

CRC16_CCITT_FALSE

CRC16_X25

CRC16_XMODEM

4.5 Power management

4.5.1 Power supply schemes

- V_{DD} = 1.65V ~ 5.5V
  External power supply for various digital and analog circuitsI. Provided externally through VDD pins.

For details about the power supply, refer to *Figure 7-3 Power system*.

4.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (BOR) circuits, which are always in working state after power-on. POR/BOR monitors the VDD supply voltage, and when the monitored supply voltage is lower than the reset threshold ($V_{POR/BOR}$), the system will enter the reset state. Users do not need to add an external hardware reset circuit.

4.5.3 Voltage regulator

The internal voltage regulator has "normal" and "low power" operating modes, and it always enabled after reset.

- The "normal" mode corresponds to a state of full speed operation.
- The "low-power" mode corresponds to some power supply working states, including Sleep and DeepSleep working modes.

4.5.4 Low-power modes

The CW32F003x3/x4 microcontrollers support two low-power modes.

- Sleep mode
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- DeepSleep mode
  DeepSleep is used to achieve the lowest power consumption, the CPU stops running, the high-speed clock modules (HSIOSC、HEX) are automatically turned off, and the low-speed clocks (LSI、RC10K、RC150K) remain unchanged.
  The device exits DeepSleep mode when an external reset, or an IWDT reset, or some peripheral interrupts.

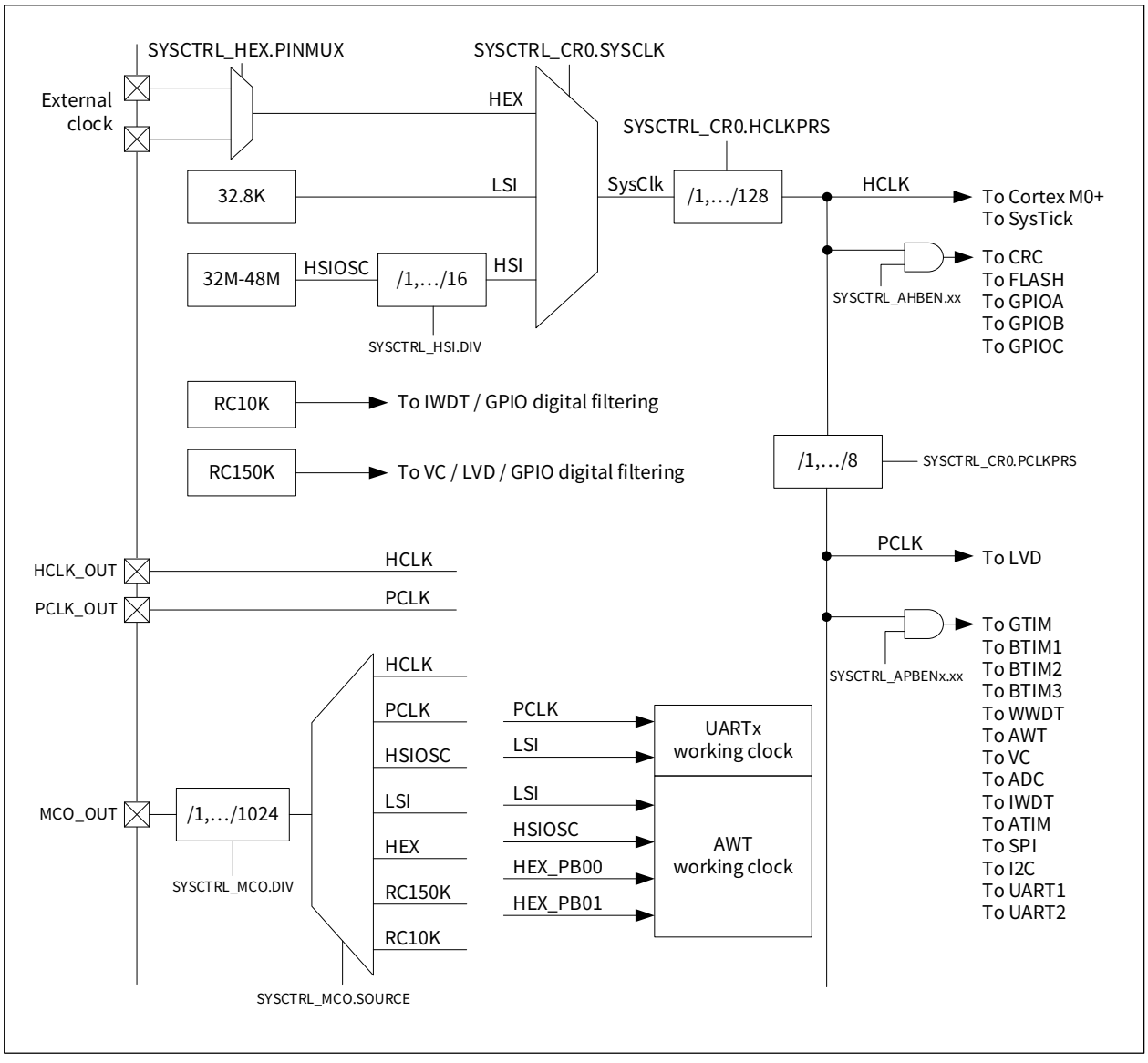
4.6 Clocks and startup

After the MCU is reset, the HSI (generated by the internal 48MHz HSIOSC oscillator frequency division) is selected as the clock source of SysClk by default, and the default value of the system clock frequency is 8MHz.The user can use the program to start the external crystal oscillator and switch the system clock source to the external clock source.

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

The internal clock tree of the system is shown below :

Figure 4-1 Clock tree of CW32F003x3/x4



4.7 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Some GPIO pins have analog functions and interface with internal analog peripherals. All I/Os can be configured as external interrupt input pins and have digital filtering.

4.8 Nested vectored interrupt controller (NVIC)

The CW32F003 family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0+) and supports programmable 4 priority levels.

- Interrupt entry vector table address can be remapped
- Closely coupled NVIC core interface
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved

This hardware block provides flexible interrupt management features with minimal interrupt latency.

4.9 Analog to digital converter (ADC)

The internal 12-bit analog to digital converter has up to 13 external and three internal (temperature sensor, voltage reference measurement, VDDA/3) channels and performs conversions in single-shot or scan modes.

In scan mode, automatic conversion is performed on a selected group of analog inputs.

High-precision voltage reference can be externally connected.

An analog watchdog feature allows very precise monitoring of the converted voltage of a selected channel. An interrupt is generated when the converted voltage is outside the programmed thresholds.

4.9.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN14 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of temperature sensor measurement, manufacturers perform individual factory calibrations for each chip. Temperature sensor factory calibration data is stored in FLASH memory.

Table 4-1 Internal temperature sensor calibration value address

ADC reference voltage	Calibration value storage address	Calibration value accuracy
Internal 1.5V	0x0010 07C6 - 0x0010 07C7	±3°C
Internal 2.5V	0x0010 07C8 - 0x0010 07C9	±3°C

4.9.2 Internal voltage reference

In addition to VDD and external reference voltage, ADC reference voltage can also choose internal reference voltage. The internal reference voltage generator (BGR) can provide stable voltage output for ADC, which is 1.5V and 2.5V respectively.

4.10 Timers and watchdogs

The CW32F003x3/x4 microcontroller integrates up to one general-purpose timer, three basic timers and one advanced control timer.

The function differences of different timers are shown in the following table:

Table 4-2 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	Capture/compare channels	Complementary outputs
Advanced control	ATIM	16-bit	Up, down, up/down	2^N(N=0,..7)	6	3
General purpose	GTIM	16-bit	Up, down, up/down	2^N(N=0,..15)	4	1
Basic	BTIM1	16-bit	Up	2^N(N=0,..15)	0	1
	BTIM2	16-bit	Up	2^N(N=0,..15)	0	1
	BTIM3	16-bit	Up	2^N(N=0,..15)	0	1

4.10.1 Advanced-control timer (ATIM)

The Advanced-control Timer (ATIM) consists of a 16-bit auto-reload counter and 7 compare units, driven by a programmable prescaler. ATIM supports 6 independent capture/compare channels, which can realize 6 independent PWM outputs or 3 pairs of complementary PWM outputs or capture 6 inputs. Can be used for basic timing/counting, measuring pulse width and period of input signals, generating output waveforms (PWM, single pulse, complementary PWM with dead time inserted, etc.).

4.10.2 General-purpose timer (GTIM)

One general-purpose timer (GTIM) is integrated inside. It includes a 16-bit automatic reloading counter and is driven by a programmable prescaler. GTIM supports 4 basic working modes: timer mode, counter mode, trigger start mode and gate control mode. It has 4 independent capture/compare channels, which can measure the pulse width of input signals (input capture) or generate output waveforms (output compare and PWM).

4.10.3 Basic timers (BTIM1..3)

Three basic timers (BTIM) are integrated inside, each BTIM is completely independent and has the same function, each contains a 16-bit automatic reloading counter and is driven by a programmable prescaler. BTIM supports four working modes: timer mode, counter mode, trigger start mode and gate control mode, and supports overflow event trigger interrupt request. Thanks to the fine processing design of the trigger signal, the BTIM can automatically perform the filtering operation of the trigger signal by the hardware, and can also cause the trigger event to generate interrupts.

4.10.4 Independent watchdog (IWDT)

The Independent Watchdog Timer (IWDT) uses a dedicated internal RC clock source, RC10K, to avoid external influences during operation. Once the IWDT is started, the user needs to reload the counter of the IWDT within a specified time interval, otherwise an overflow will trigger a reset or generate an interrupt signal. After the IWDT is started, the counting can be stopped. The user can choose to keep the IWDT running or suspend counting while in Deep Sleep mode.

A specially set key-value register can lock the key registers of the IWDT to prevent the registers from being accidentally modified.

4.10.5 System window watchdog (WWDT)

The CW32F003x3/x4 microcontroller integrates a window watchdog timer (WWDT), the user needs to refresh within the set time window, otherwise the watchdog overflow will trigger a system reset. WWDT is usually used to monitor the program execution flow with strict time requirements to prevent the abnormal execution of the application program caused by external interference or unknown conditions, resulting in system failure.

4.10.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0

4.11 Inter-integrated circuit interfaces (I2C)

The I2C controller can serially send the data to be sent to the I2C bus according to the I2C specification according to the set transmission rate (standard, fast, high-speed), and detect the state during the communication process. I2C also support bus conflict and arbitration handling in multi-master communication.

The main features of the I2C controller are:

- Supports master send/receive and slave send/receive four working modes
- Supports clock stretching (clock synchronization) and multi-master communication collision arbitration
- Supports standard (100Kbps)/fast (400Kbps)/high speed (1Mbps) three working rates
- Supports 7-bit addressing mode
- Supports 3 slave addresses
- Supports broadcast address
- Supports input signal noise filtering function
- Supports interrupt status query function

4.12 Universal asynchronous receiver/transmitter (UART)

Universal asynchronous receiver/transmitter (UART) supports asynchronous full-duplex, synchronous half-duplex and single-wire half-duplex modes, supports hardware data flow control and multi-machine communication; the data frame structure is programmable, and a wide range of baud rate selection can be provided through the fractional baud rate generator.

The UART controller works in a dual clock domain, allowing data reception in deep sleep mode, and the reception completion interrupt can wake the MCU back to Active mode.

4.13 Serial peripheral interface (SPI)

Serial Peripheral Interface (SPI) supports bidirectional full-duplex, single-wire half-duplex and simplex communication modes, MCU can be configured as master or slave, multi-master communication mode is supported.

The main features of the Serial Peripheral Interface (SPI) are:

- Supports master mode, slave mode
- Supports full-duplex, single-wire half-duplex, simplex
- 4-bit to 16-bit selectable data frame width
- Supports sending and receiving data LSB or MSB first
- Clock Polarity and Clock Phase is programmable
- Communication rates up to PCLK/2 in master mode
- Communication rates up to PCLK/4 in slave mode
- Supports multi-machine communication mode
- 8 interrupt sources with flag bits

4.14 Serial wire debug port (SWD)

An ARM SWD interface is provided, and users can use the CW-DPLINK of Xinyuan Semiconductor to connect to the MCU to debug and simulate in the IDE development environment.

5 Pin descriptions

Figure 5-1 TSSOP24 package pinout (top view)

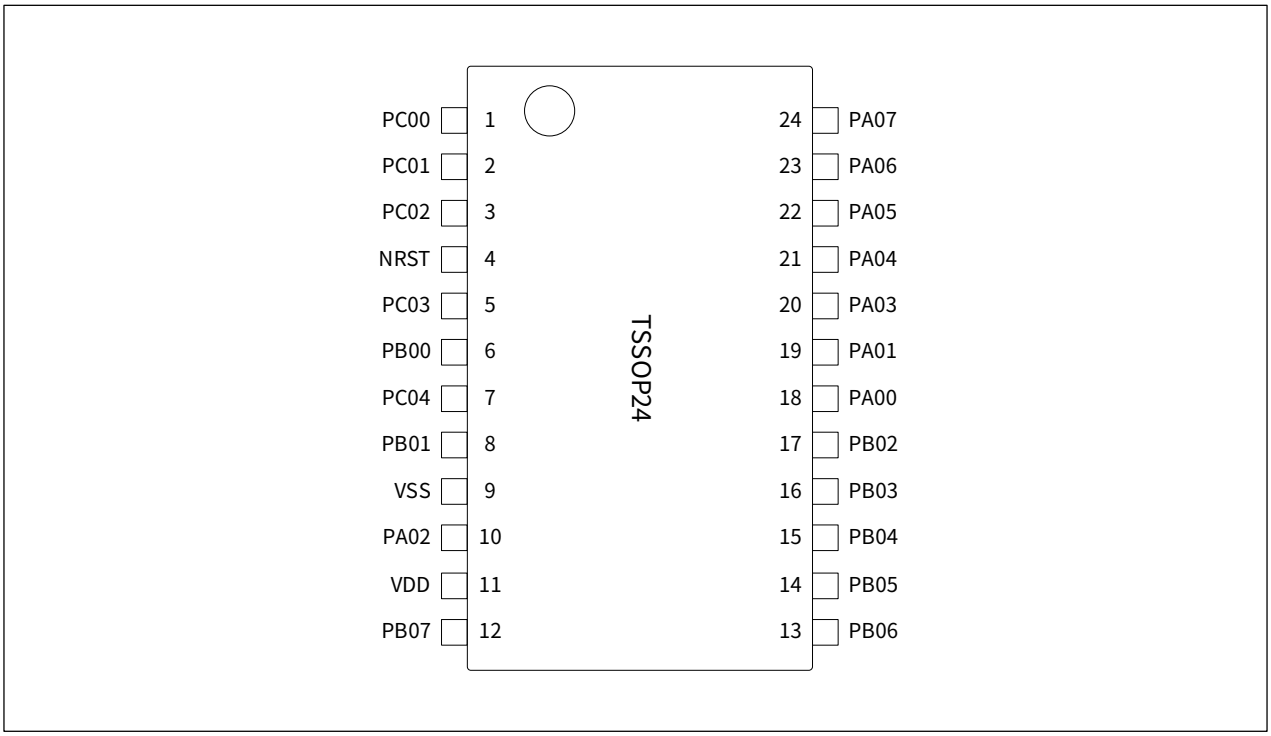


Figure 5-2 TSSOP20 package pinout (top view)

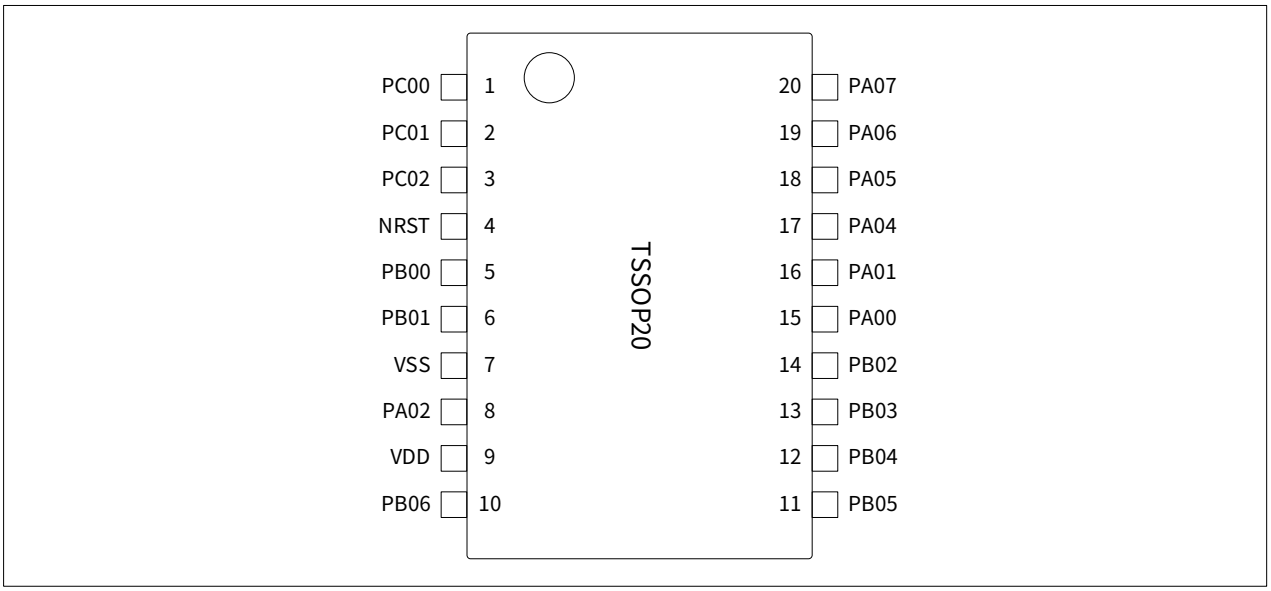


Figure 5-3 QFN20 package pinout (top view)

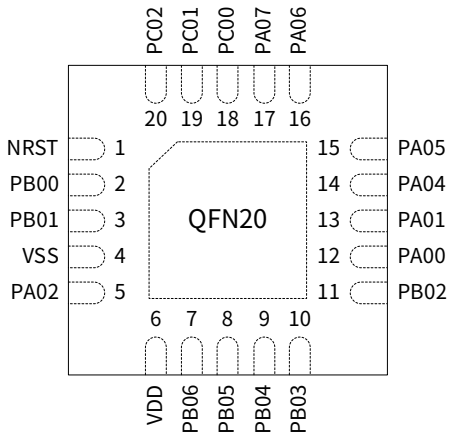


Table 5-1 Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	TTa	Connect the I/O port for the analog function
	TC	Standard I/ O pin
	RST	Reset input pin
Notes	Unless otherwise specified by a note, all pins are set as high impedance input state after reset	
Additional functions	Digital function	Functions selected through GPIOx_AFRL registers
	Analog function	Functions directly selected through peripheral registers

Table 5-2 CW32F003x3/x4 pin definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
TSSOP24	TSSOP20	QFN20					Digital function	Analog function
1	1	18	PC00	I/O	TTa	-	UART2_RXD, UART1_TXD, SPI_SCK, ATIM_CH1A, GTIM_CH2, BTIM1_TOGP, HCLK_OUT	ADC_AIN5, VC2_CH6
2	2	19	PC01	I/O	TTa	-	UART2_TXD, GTIM_ETR, SPI_MISO, ATIM_CH2A, GTIM_CH3, BTIM1_TOGN, VC1_OUT	ADC_AIN6, VC2_CH7
3	3	20	PC02	I/O	TTa	-	UART2_RXD, IR_OUT, SPI_MOSI, ATIM_CH3A, GTIM_CH4, HCLK_OUT, AWT_ETR	ADC_AIN7, VC1_CH0
4	4	1	PC05/ NRST	I/O	RST	-	By default, it is the device reset input, it can also be used as a GPIO port, please refer to SYSCTRL_CR2.RSTIO bit field	
5	-	-	PC03	I/O	TC	-	UART1_TXD, SPI_CS, SPI_MISO, ATIM_CH3B, GTIM_CH3, GTIM_TOGP, ATIM_BK	
6	5	2	PB00	I/O	TTa	-	UART1_RXD, I2C_SDA, SPI_CS, ATIM_CH1B, GTIM_CH1, GTIM_TOGP, AWT_ETR	ADC_AIN8, VC1_CH1, HEX_PB00
7	-	-	PC04	I/O	TC	-	UART1_RXD, IR_OUT, SPI_MOSI, ATIM_CH2B, GTIM_CH4, GTIM_TOGN	
8	6	3	PB01	I/O	TTa	-	UART1_TXD, LVD_OUT, I2C_SCL, ATIM_BK, GTIM_CH2, GTIM_TOGN, AWT_ETR	ADC_AIN9, VC1_CH2, HEX_PB01
9	7	4	VSS	S	-	-	Ground	
10	8	5	PA02/ SWDIO	I/O	TC	1	UART1_RXD, UART2_TXD, I2C_SDA, GTIM_ETR, GTIM_CH3, VC2_OUT, AWT_ETR	
11	9	6	VDD	S	-	-	Power supply	
12	-	-	PB07	I/O	TC	-	UART2_RXD, UART1_TXD, SPI_SCK, GTIM_CH1, BTIM2_TOGN, BTIM_ETR	
13	10	7	PB06	I/O	TTa	-	UART1_TXD, I2C_SCL, SPI_CS, ATIM_CH1A, GTIM_TOGP, BTIM2_TOGP, HCLK_OUT	ADC_AIN10, LVD_CH1

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Additional functions	
TSSOP24	TSSOP20	QFN20					Digital function	Analog function
14	11	8	PB05	I/O	TTa	-	UART1_RXD, I2C_SDA, BTIM_ETR, ATIM_CH1B, GTIM_TOGN, BTIM2_TOGN, ATIM_BK	ADC_AIN11, VC1_CH3
15	12	9	PB04	I/O	TTa	-	UART2_TXD, I2C_SCL, GTIM_ETR, ATIM_ETR, GTIM_CH1, BTIM3_TOGN, ATIM_BK	ExRef, VC1_CH4
16	13	10	PB03	I/O	TTa	-	UART2_RXD, I2C_SDA, PCLK_OUT, ATIM_CH2A, GTIM_CH2, BTIM3_TOGP, IR_OUT	ADC_AIN12, VC1_CH5, LVD_CH2
17	14	11	PB02	I/O	TTa	-	UART1_TXD, UART2_CTS, SPI_CS, ATIM_CH2B, GTIM_CH3, BTIM1_TOGP, MCO_OUT	ADC_AIN0, VC1_CH6, VC2_CH0
18	15	12	PA00	I/O	TTa	-	UART1_RXD, UART2_RTS, SPI_SCK, ATIM_CH3A, GTIM_CH4, BTIM1_TOGN, VC1_OUT	VC1_CH7, VC2_CH1, LVD_CH3
19	16	13	PA01	I/O	TTa	-	UART2_TXD, VC2_OUT, SPI_MOSI, ATIM_CH3B, GTIM_CH1, BTIM2_TOGP, MCO_OUT	ADC_AIN1, VC2_CH2
20	-	-	PA03	I/O	TC	-	UART2_TXD, UART1_RXD, PCLK_OUT, ATIM_BK, GTIM_ETR, BTIM2_TOGP, LVD_OUT	
21	17	14	PA04	I/O	TTa	-	UART1_RXD, IR_OUT, SPI_MISO, ATIM_CH3B, GTIM_CH2, BTIM2_TOGN, GTIM_ETR	ADC_AIN2, VC2_CH3
22	18	15	PA05/ SWCLK	I/O	TTa	1	UART1_TXD, UART2_RXD, I2C_SCL, GTIM_CH4, BTIM_ETR, MCO_OUT	
23	19	16	PA06	I/O	TTa	-	UART1_CTS, UART2_TXD, I2C_SDA, ATIM_CH2B, GTIM_CH3, BTIM3_TOGP, LVD_OUT	ADC_AIN3, VC2_CH4
24	20	17	PA07	I/O	TTa	-	UART1_RTS, UART2_RXD, VC1_OUT, ATIM_CH1B, GTIM_CH4, BTIM3_TOGN, ATIM_BK	ADC_AIN4, VC2_CH5

Caution 1: After reset, these pins are configured as SWDIO and SWCLK functions, and the internal pull-up resistors are turned on by default.

Table 5-3 Alternate functions selected through GPIOA_AFRL registers for port A

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA00	UART1_RXD	UART2_RTS	SPI_SCK	ATIM_CH3A	GTIM_CH4	BTIM1_TOGN	VC1_OUT
PA01	UART2_TXD	VC2_OUT	SPI_MOSI	ATIM_CH3B	GTIM_CH1	BTIM2_TOGP	MCO_OUT
PA02/SWDIO	UART1_RXD	UART2_TXD	I2C_SDA	GTIM_ETR	GTIM_CH3	VC2_OUT	AWT_ETR
PA03	UART2_TXD	UART1_RXD	PCLK_OUT	ATIM_BK	GTIM_ETR	BTIM2_TOGP	LVD_OUT
PA04	UART1_RXD	IR_OUT	SPI_MISO	ATIM_CH3B	GTIM_CH2	BTIM2_TOGN	GTIM_ETR
PA05/SWCLK	UART1_TXD	UART2_RXD	I2C_SCL		GTIM_CH4	BTIM_ETR	MCO_OUT
PA06	UART1_CTS	UART2_TXD	I2C_SDA	ATIM_CH2B	GTIM_CH3	BTIM3_TOGP	LVD_OUT
PA07	UART1_RTS	UART2_RXD	VC1_OUT	ATIM_CH1B	GTIM_CH4	BTIM3_TOGN	ATIM_BK

Table 5-4 Alternate functions selected through GPIOB_AFRL registers for port B

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB00	UART1_RXD	I2C_SDA	SPI_CS	ATIM_CH1B	GTIM_CH1	GTIM_TOGP	AWT_ETR
PB01	UART1_TXD	LVD_OUT	I2C_SCL	ATIM_BK	GTIM_CH2	GTIM_TOGN	AWT_ETR
PB02	UART1_TXD	UART2_CTS	SPI_CS	ATIM_CH2B	GTIM_CH3	BTIM1_TOGP	MCO_OUT
PB03	UART2_RXD	I2C_SDA	PCLK_OUT	ATIM_CH2A	GTIM_CH2	BTIM3_TOGP	IR_OUT
PB04	UART2_TXD	I2C_SCL	GTIM_ETR	ATIM_ETR	GTIM_CH1	BTIM3_TOGN	ATIM_BK
PB05	UART1_RXD	I2C_SDA	BTIM_ETR	ATIM_CH1B	GTIM_TOGN	BTIM2_TOGN	ATIM_BK
PB06	UART1_TXD	I2C_SCL	SPI_CS	ATIM_CH1A	GTIM_TOGP	BTIM2_TOGP	HCLK_OUT
PB07	UART2_RXD	UART1_TXD	SPI_SCK		GTIM_CH1	BTIM2_TOGN	BTIM_ETR

Table 5-5 Alternate functions selected through GPIOC_AFRL registers for port C

Pin name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC00	UART2_RXD	UART1_TXD	SPI_SCK	ATIM_CH1A	GTIM_CH2	BTIM1_TOGP	HCLK_OUT
PC01	UART2_TXD	GTIM_ETR	SPI_MISO	ATIM_CH2A	GTIM_CH3	BTIM1_TOGN	VC1_OUT
PC02	UART2_RXD	IR_OUT	SPI_MOSI	ATIM_CH3A	GTIM_CH4	HCLK_OUT	AWT_ETR
PC03	UART1_TXD	SPI_CS	SPI_MISO	ATIM_CH3B	GTIM_CH3	GTIM_TOGP	ATIM_BK
PC04	UART1_RXD	IR_OUT	SPI_MOSI	ATIM_CH2B	GTIM_CH4	GTIM_TOGN	

6 Address mapping

Figure 6-1 CW32F003x3/x4 internal address mapping

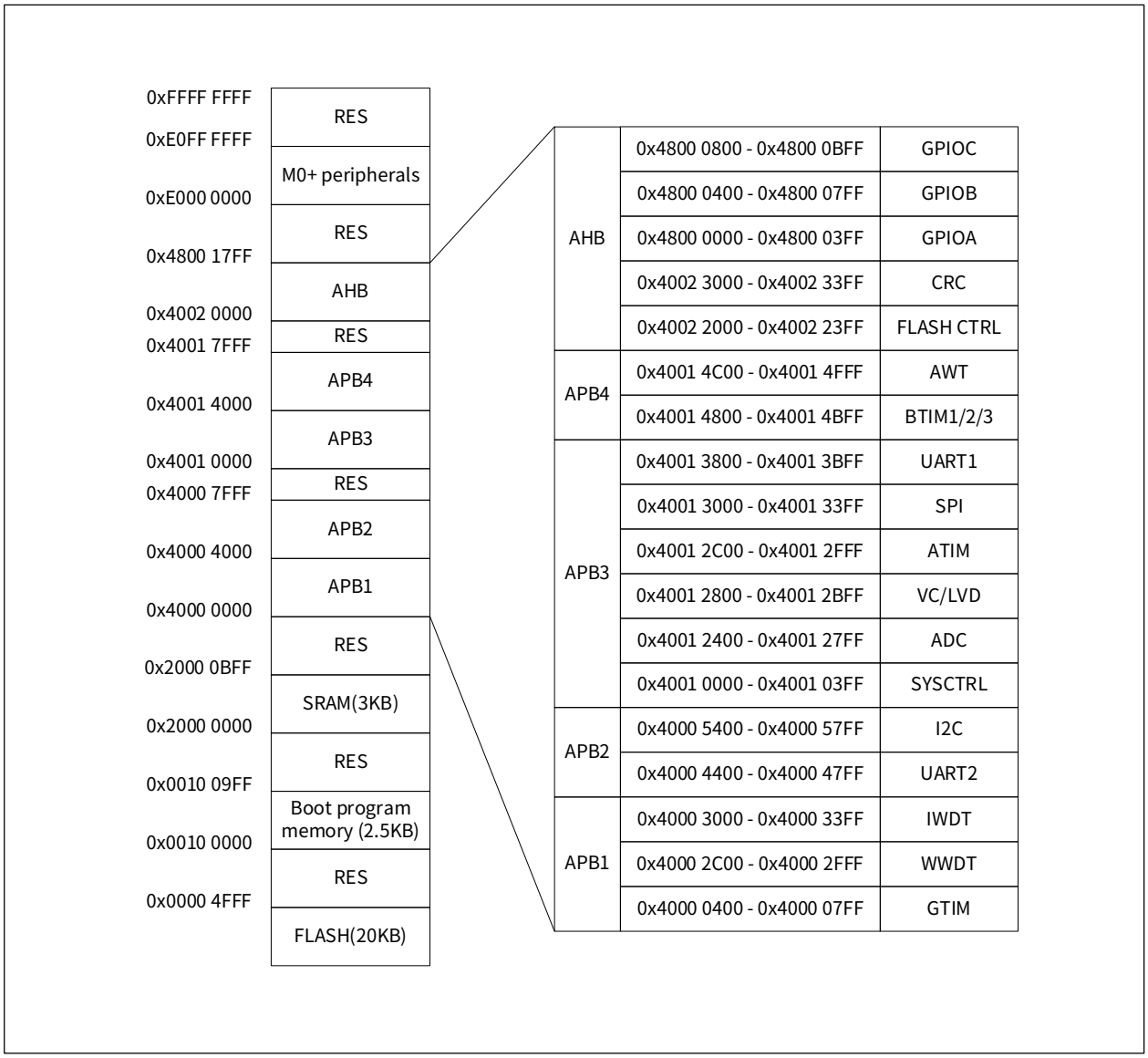


Table 6-1 CW32F003x3/x4 peripheral register boundary addresses

Device or bus	Boundary address	Size	Peripheral
Main FLASH memory	0x0000 0000 - 0x0000 4FFF	20KB	Main FLASH
OTP memory	0x0010 0770 - 0x0010 0785	22B	OTP
Boot program memory	0x0010 0000 - 0x0010 09FF	2.5KB	BootLoader
SRAM memory	0x2000 0000 - 0x2000 0BFF	3KB	SRAM
APB1 peripheral	0x4000 0400 - 0x4000 07FF	1KB	GTIM
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDT
	0x4000 3000 - 0x4000 33FF	1KB	IWDT
APB2 peripheral	0x4000 4400 - 0x4000 47FF	1KB	UART2
	0x4000 5400 - 0x4000 57FF	1KB	I2C
APB3 peripheral	0x4001 0000 - 0x4001 03FF	1KB	SYSCTRL
	0x4001 2400 - 0x4001 27FF	1KB	ADC
	0x4001 2800 - 0x4001 2BFF	1KB	VC/LVD
	0x4001 2C00 - 0x4001 2FFF	1KB	ATIM
	0x4001 3000 - 0x4001 33FF	1KB	SPI
	0x4001 3800 - 0x4001 3BFF	1KB	UART1
APB4 peripheral	0x4001 4800 - 0x4001 4BFF	1KB	BTIM1/2/3
	0x4001 4C00 - 0x4001 4FFF	1KB	AWT
AHB peripheral	0x4002 2000 - 0x4002 23FF	1KB	FLASH CTRL
	0x4002 3000 - 0x4002 33FF	1KB	CRC
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
M0+ peripheral	0xE000 0000 - 0xE00F FFFF	1MB	M0+ peripheral

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3Σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C and V_{DD} = 3.3V. They are given only as design guidelines and are not tested.

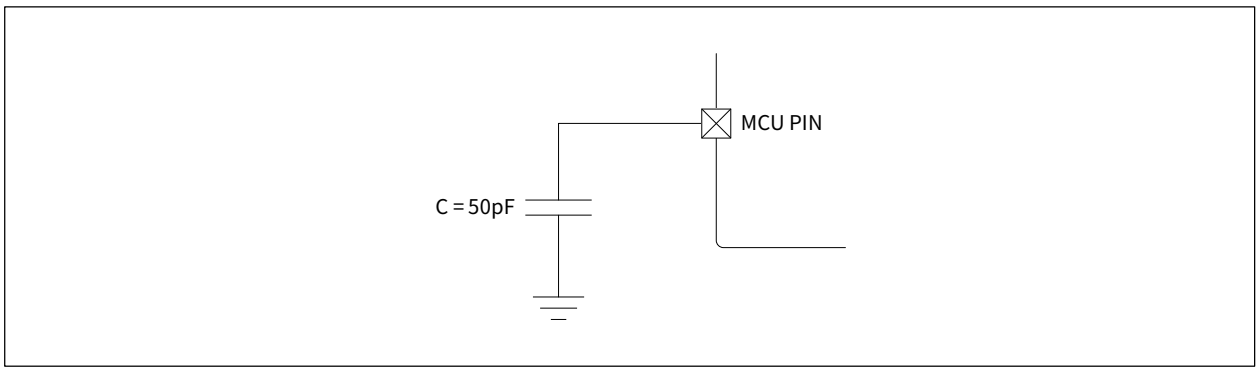
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below:

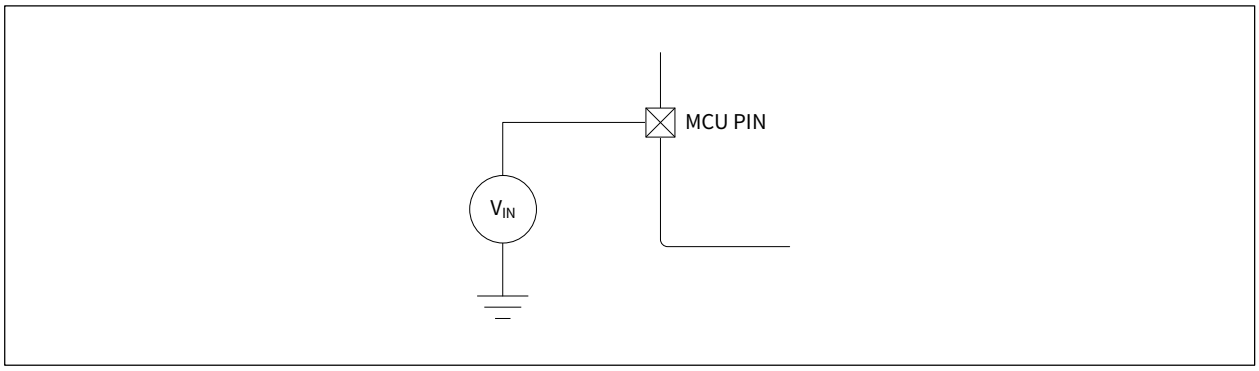
Figure 7-1 Pin loading conditions



7.1.5 Pin input voltage

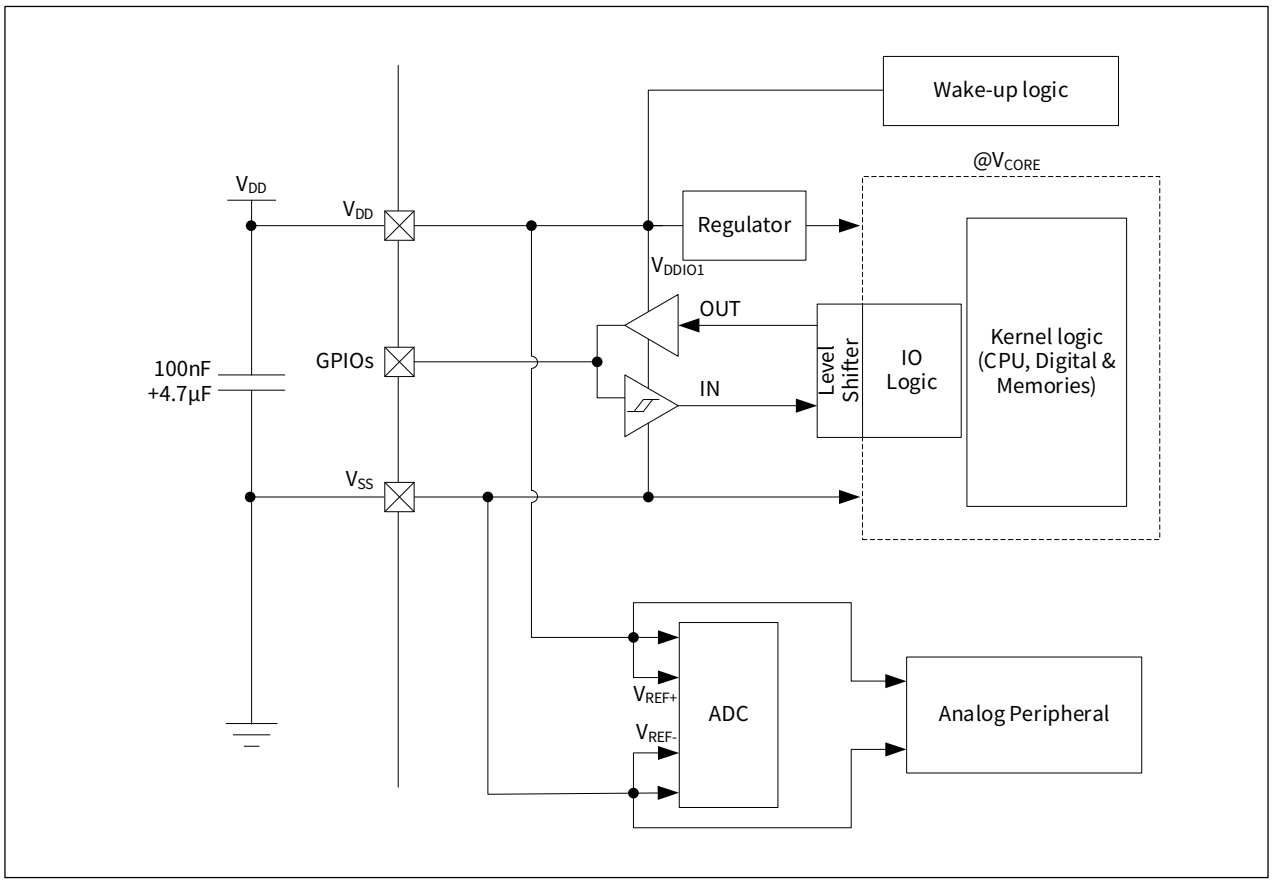
The input voltage measurement on a pin of the device is described in the figure below:

Figure 7-2 Pin input voltage



7.1.6 Power system

Figure 7-3 Power system

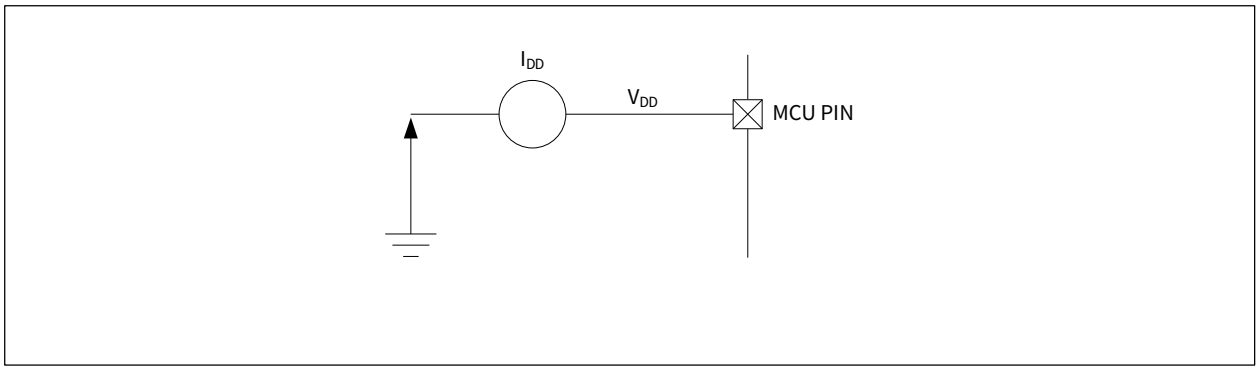


Caution 1: Each power supply pair (V_{DD}/V_{SS}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Caution 2: All V_{DD} pins must be powered and at the same voltage.

7.1.7 Current consumption measurement

Figure 7-4 Method of measurement



7.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 7-1, Table 7-2 and Table 7-3 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7-1 Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DD} - V_{SS}	External main supply voltage	-0.3	6.0	V
V_{IN} [1]	Input voltage on port IO	V_{SS} - 0.3	V_{DD} + 0.3	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	*See Table 7-20 ESD characteristics*		kV

Caution 1: V_{IN} maximum must always be respected, refer to Table 7-2 for the maximum allowable injection current value.

Table 7-2 Current characteristics

Symbol	Ratings	Max.	Unit
$I_{VDD(PIN)}$	Total current into sum of V_{DD} power lines (source)	+100	mA
$I_{VSS(PIN)}$	Total current out of sum of all V_{SS} power lines (sink)	-100	
$I_{IO(PIN)}$	Current into a single I/O or control pin	+25	
	Current out of a single I/O or control pin	-25	
$I_{IO(PIN)}$	Current into a single I/O or control pin[4]	+50	
	Current out of a single I/O or control pin[4]	-50	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os or control pins	+80	
	Total output current sourced by sum of all I/Os or control pins	-80	
$I_{INJ(PIN)}$ [1、2]	Injected current on TC and RST pins	±5	
	Injected current on TTa pins	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) [3]	±25	

Caution 1: $I_{INJ(PIN)}$ must not exceed its limit to ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed to not to exceed its maximum value, also ensure that external limit $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. When $V_{IN}>V_{DD}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.

Caution 2: Negative injection disturbs the analog performance of the device.

Caution 3: When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents. This result is based on the characterization of the maximum value of $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Caution 4: Only applies to the special pins of the TSSOP20 package and TSSOP20 package: PA04, PB00, PB01, PB06.

Table 7-3 Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	125	

7.3 Operating conditions

7.3.1 General operating conditions

Table 7-4 General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB bus fre-quency	$V_{DD} \geqslant 1.8V$	0	48	MHz
f_{PCLK}	Internal APB bus fre-quency	$V_{DD} \geqslant 1.8V$	0	48	
f_{HCLK}	Internal AHB bus fre-quency	$1.65V \leqslant V_{DD} < 1.8V$	0	24	
f_{PCLK}	Internal APB bus fre-quency	$1.65V \leqslant V_{DD} < 1.8V$	0	24	
V_{DD}	Standard operating voltage	-	1.65	5.5	V
V_{IN}	I/O input voltage	TC I/O	-0.3	$V_{DD}+0.3$	V
		TTa I/O	-0.3	$V_{DD}+0.3$	
P_D	Power dissipation at T_A= 105°C for suffix 7 [1]	TSSOP20	-	263	mW
		QFN20	-	220	
T_A	Ambient temperature (suffix 7 version)	Maximum power dissipation	-40	105	°C
		Low power dissipation [2]	-40	125	
T_J	Junction temperature range	Suffix 7 version	-40	125	°C

Caution 1: If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}(See 8.4 Thermal characteristics).

Caution 2: In low power dissipation state, $T_A$can be extended to this range as long as T_J does not exceed T_{Jmax}(See 8.4 Thermal characteristics).

7.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are tested under the working conditions listed in *Table 7-4 General operating conditions*.

Table 7-5 Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	μs/V
	V_{DD} fall time rate		20	∞	

7.3.3 Embedded reset and power control block

The parameters given in the table below are tested under the working conditions listed in *Table 7-4 General operating conditions*.

Table 7-6 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{POR/BOR}$	Power on/power down reset threshold	Falling edge	1.45 [1]	1.50	1.55 [2]	V
		Rising edge	1.50 [2]	1.55	1.60	V
$V_{BORhyst}$ [3]	BOR hysteresis	-	-	50	-	mV
$t_{RSTTEMPO}$ [3]	Reset temporization	-	2	2.50	3	ms

Caution 1: The product behavior is guaranteed by design down to the minimum$V_{POR/BOR}$ value.

Caution 2: Data based on characterization results, not tested in production.

Caution 3: Guaranteed by design, not tested in production.

7.3.4 Internal reference voltage

Table 7-7 Internal reference voltage

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{REFINT1V5}$	Internal 1.5V reference voltage	-40°C < T_A < +105°C	1.485	1.50	1.515	V
$V_{REFINT2V5}$	Internal 2.5V reference voltage	-40°C < T_A < +105°C	2.475	2.50	2.525	V
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3V	-	-	10 [1]	mV
T_{Coeff}	Temperature coefficient	-	-60 [1]	-	+60 [1]	ppm/°C

Caution 1: Guaranteed by design, not tested in production.

7.3.5 Supply current characteristics

Current consumption is affected by many factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

Figure 7-4 Method of measurement shows the circuit for testing current consumption.

All result of the Run-mode current consumption measurements based on the same limited code used to test CoreMark.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency
  - 0 wait state inserted when 0 to 24 MHz
  - 1 wait state inserted when above 24 MHz
  - 2 wait state inserted when above 48 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The data given in Table 7-8 to Table 7-9 are derived from tests performed under the ambient temperature and supply voltage noted in the remarks. For the test conditions, please refer to *Table 7-4 General operating conditions*.

Table 7-8 Typical and maximum current consumption at V_{DD} = 5.5V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled		Unit
				Typ.	Max.[1] T_A = 105°C	
I_{DD}	Supply current in Active mode, code executing from Flash	HSI clock	48MHz	5.5	6	mA
			24MHz	4	4.5	
I_{DD}	Supply current in Active mode, code executing from RAM	HSI clock	48MHz	4.5	5	mA
			24MHz	2.5	3	
I_{DD}	Supply current in Sleep mode, code executing from Flash or RAM	HSI clock	48MHz	3	3.5	mA
			24MHz	1.8	2.2	

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.

Table 7-9 Typical and maximum current consumption in DeepSleep

Symbol	Parameter	Conditions	Typ. @V_{DD} (V_{DD} = V_{DDA})	Max.[1]	Unit
			3.6V	T_A=105°C	
I_{DD}[2]	Supply current in DeepSleep mode	The regulator is in Active mode, all oscillators are off	22	42	μA
		The regulator is in Active mode, LSI and IWDT are on	24	45	

Caution 1: Data based on characterization results, not tested in production unless otherwise specified.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = 3.3V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency
  - 0 wait state inserted when 0 to 24MHz
  - 1 wait state inserted when above 24MHz
  - 2 wait state inserted when above 48MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Table 7-10 Typical current consumption in Active mode, program running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Active mode	Runs from FLASH with 48MHz internal HSIOSC clock	48MHz	5.5	3.5	mA
			8MHz	1.7	1.5	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

- I/O static current consumption

  All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up resistors values given in *Table 7-21 I/O static characteristics*.

  For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

  If the input voltage level of the I/Os is the intermediate voltage level, it will continuously cause the internal Schmitt trigger to flip, resulting in additional random current consumption (although it is small). If it is required to judge the level flip situation in real time, that should configure the I/Os in analog input mode to avoid this.

Caution 1: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. T o avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

- I/O dynamic current consumption

  In addition to the internal peripheral current consumption measured previously, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

  where:

  I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

  V_{DDIOx} is the I/O supply voltage

  f_{SW} is the I/O switching frequency

  C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

  C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 7-11 Switching output I/O current consumption

Symbol	Parameter	Conditions [1]	I/O toggling frequency (f_{SW})	Typ.	Unit
I_{SW}	I/O current consumption	V_{DDIOx} = 3.3V C_{EXT} = 0pF $C = C_{INT} + C_{EXT} + C_S$	4MHz	0.18	mA
			8MHz	0.37	
			16MHz	0.76	
			24MHz	1.39	
		V_{DDIOx} = 3.3V C_{EXT} = 22pF $C = C_{INT} + C_{EXT} + C_S$	4MHz	0.49	
			8MHz	0.94	
			16MHz	2.38	
			24MHz	3.99	
		V_{DDIOx} = 3.3V C_{EXT} = 47pF $C = C_{INT} + C_{EXT} + C_S$	4MHz	0.81	
			8MHz	1.7	
			16MHz	3.67	

Caution 1: C_S = 7pF (estimated value).

7.3.6 Wakeup time from low-power mode

The wakeup times given in the table below are tested during the wake-up phase of the HSIOSC.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from DeepSleep mode, SYSCLK takes the default setting: HSI 4MHz.

All test environments are from ambient temperature and supply voltage conditions summarized in *Table 7-4 General operating conditions*.

Table 7-12 Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ. @V_{DD} (V_{DD} = V_{DDA})	Max.	Unit
			3.3V		
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4	-	HCLK
t_{WUDEEP}	Wakeup form DeepSleep mode	Regulator in Active mode	4.0	5.0	µs

7.3.7 External clock source characteristics

External clock signal from PB00/PB01 pins to be input to HEX circuit is allowed.

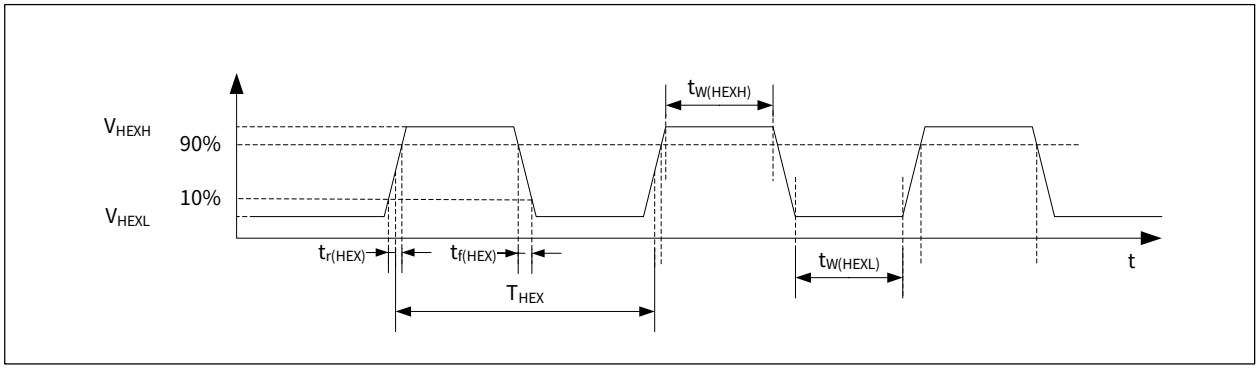
The external clock signal has to respect the I/O characteristics in Section *7.3.11 I/O port characteristics*. The recommended clock input waveform is shown in *Figure 7-5 External clock source AC timing diagram*.

Table 7-13 External clock input characteristics

Symbol	Parameter [1]	Min.	Typ.	Max.	Unit
f_{HEX_EXT}	User external clock source frequency	1	-	32	MHz
V_{HEXH}	External clock input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HEXL}	External clock input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{W(HEXH)}$ $t_{W(HEXL)}$	External clock high or low time	15	-	-	ns
$t_{r(HEX)}$ $t_{f(HEX)}$	External clock rise or fall time	-	-	20	

Caution 1: Guaranteed by design, not tested in production.

Figure 7-5 External clock source AC timing diagram



7.3.8 Internal clock source characteristics

The data given in the following table is based on the sample tests of the test environment indicated by *Table 7-4 General operating conditions*.

High-speed internal (HSIOSC) RC oscillator

Table 7-14 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
TRIM	HSI user trimming step	-	-	0.2	-	%
$Duty_{HSI}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = -40°C ~ +105°C	-2.0	-	+2.0	%
		T_A = +25°C	-0.5	-	+0.5	%
$t_{SU(HSI)}$	HIS oscillator startup time	-	3	-	5	μs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	600	-	μA

Low-speed internal (LSI) RC oscillator

Table 7-15 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	-	32.8	-	kHz
TRIM	LSI user trimming step	-	-	1	-	%
$Duty_{LSI}$	Duty cycle	-	45	-	55	%
ACC_{LSI}	Accuracy of the LSI oscillator (factory calibrated)	T_A = -40°C ~ +105°C	-3	-	+3	%
		T_A = +25°C	-1	-	+1	%
$t_{SU(LSI)}$	LSI oscillator startup time	-	-	-	50	μs
$I_{DDA(LSI)}$	LSI oscillator power consumption	-	-	1	-	μA

Ultra-Low-Speed Internal (RC10K) RC Oscillator

Table 7-16 RC10K oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{RC10K}	Frequency	-	-	8	-	kHz
$Duty_{RC10K}$	Duty cycle	-	45	-	55	%
ACC_{RC10K}	Accuracy of the RC10K oscillator(factory calibrated)	T_A = -40°C ~ +105°C	-50	-	+50	%
		-	-20	-	+20	%

Mid-low-speed internal (RC150K) RC oscillator

Table 7-17 RC150K oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{RC150K}	Frequency	-	-	120	-	kHz
$Duty_{RC150K}$	Duty cycle	-	45	-	55	%
ACC_{RC150K}	Accuracy of the RC150K oscillator(factory calibrated)	T_A = -40°C ~ +105°C	-50	-	+50	%
		T_A = +25°C	-20	-	+20	%

7.3.9 Memory characteristics

Flash memory

The characteristics are for -40 to +105 °C test environment unless otherwise specified.

Table 7-18 FLASH memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max. [1]	Unit
t_{prog8}	8-bit programming time	T_A = -40°C ~ +105°C	-	31	-	μs
t_{prog16}	16-bit programming time	T_A = -40°C ~ +105°C	-	37	-	μs
t_{prog32}	32-bit programming time	T_A = -40°C ~ +105°C	-	53	-	μs
t_{ERASE}	Page erase time	T_A = -40°C ~ +105°C	-	4.5	-	ms
t_{ME}	Mass erase time	T_A = -40°C ~ +105°C	-	40	-	ms
I_{DD}	Supply current	Write mode	-	-	3.5	mA
		Erase mode	-	-	2.0	mA
V_{prog}	Programming voltage	-	1.65	-	5.5	V

Caution 1: Guaranteed by design, not tested in production.

Table 7-19 FLASH memory endurance and data retention

Symbol	Parameter	Conditions	Min. [1]	Unit
N_{NED}	Endurance	T_A = -40°C ~ +105°C	20000	Times
t_{RET}	Data retention	T_A = 25°C	100	Years
		T_A = 85°C	25	
		T_A = 105°C	10	

Caution 1: Obtained by comprehensive evaluation, not tested in production.

7.3.10 ESD characteristics

Use specific measurement methods to test the strength of the chip to determine its electrical sensitivity performance.

Table 7-20 ESD characteristics

Symbol	Parameter	Condition	Typ.	Max.	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C , conforming to JESD22-A115C	-	8	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C , conforming to JESD22-A115C	-	2	

7.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-21 I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	0.3 V_{DDIOx}	V
V_{IH}	High level input voltage	TC and TTa I/O	0.7 V_{DDIOx}	-	-	V
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	400 [1]	-	mV
I_{ikg}	Input leakage current	TC and TTa I/O in digital mode $V_{SS} \leqslant V_{IN} \leqslant V_{DDIOx}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DDIOx} \leqslant V_{IN} \leqslant V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \leqslant V_{IN} \leqslant V_{DDA}$	-	-	±0.2	
R_{PU} [2]	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	50	80	180	kΩ
R_{PD} [2]	Weak pull-down equivalent resistor	$V_{IN} = V_{DDIOx}$	20	30	45	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Caution 1: Data based on design simulation only. Not tested in production.

Caution 2: Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal.

Output driving current

The GPIOs can sink or source up to ±8mA, and sink or source up to ±20mA with a relaxed V_{OH} and V_{OL}.

n the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *7.2 Absolute maximum ratings*.

- The sum of the currents sourced by all the I/Os on V_{DDIOx} , plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (See *Table 7-1 Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (See *Table 7-1 Voltage characteristics*).

Output voltage levels

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

All I/Os are designed as CMOS- and TTL-compliant.

Table 7-22 Special pin output voltage characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	High-level output voltage source current	Sourcing 10mA, V_{DD} = 3.3V	3.15	-	V
		Sourcing 20mA, V_{DD} = 3.3V	2.95	-	
V_{OL}	Low-level output voltage sink current	Sinking 10mA, V_{DD} = 3.3V	-	0.10	
		Sinking 20mA, V_{DD} = 3.3V	-	0.22	

Caution 1: The above table only applies to the special pins of the TSSOP20 package and TSSOP20 package: PA04、PB00、PB01、PB06.

Table 7-23 General output voltage characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	High-level output voltage source current	Sourcing 10mA, V_{DD} = 3.3V	3.00	-	V
		Sourcing 20mA, V_{DD} = 3.3V	2.72	-	
V_{OL}	Low-level output voltage sink current	Sinking 10mA, V_{DD} = 3.3V	-	0.22	
		Sinking 20mA, V_{DD} = 3.3V	-	0.42	

Input/output AC characteristics

The values and definitions of the AC characteristics of the I/Os are given by the following charts respectively.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

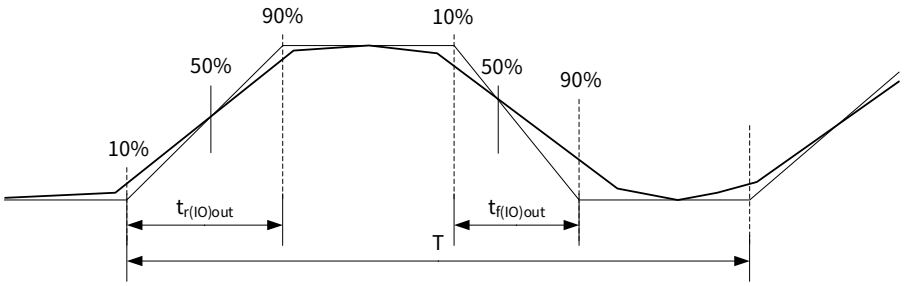
Table 7-24 I/O AC characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$f_{max(IO)out}$	Maximum frequency [2]	C_L = 30pF, $V_{DDIOx} \geqslant$ 2.7V	-	50	MHz
		C_L = 50pF, $V_{DDIOx} \geqslant$ 2.7V	-	30	
		C_L = 50pF, 2.4V $\leqslant V_{DDIOx} <$ 2.7V	-	20	
$t_{f(IO)out}$	Output fall time	C_L = 30pF, $V_{DDIOx} \geqslant$ 2.7V	-	5	ns
		C_L = 50pF, $V_{DDIOx} \geqslant$ 2.7V	-	8	
		C_L = 50pF, 2.4V $\leqslant V_{DDIOx} <$ 2.7V	-	12	
$t_{r(IO)out}$	Output rise time	C_L = 30pF, $V_{DDIOx} \geqslant$ 2.7V	-	5	
		C_L = 50pF, $V_{DDIOx} \geqslant$ 2.7V	-	8	
		C_L = 50pF, 2.4V $\leqslant V_{DDIOx} <$ 2.7V	-	12	

Caution 1: Data based on design simulation only, not tested in production.

Caution 2: The maximum frequency is defined in the figure below

Figure 7-6 I/O AC characteristics definition



Maximum frequency is achieved if ($t_r + t_f$) $\leqslant$ 2/3T and if the duty cycle is (45-55%) when loaded by C_L

7.3.12 NRST pin characteristics

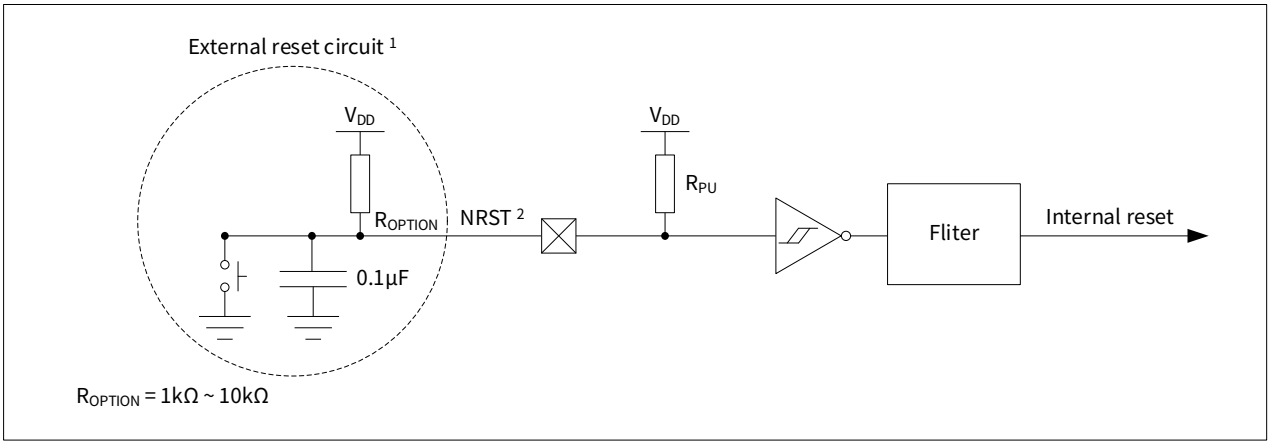
The NRST pin is connected to a permanent pull-up resistor R_{PU} internally.

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

Table 7-25 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3V_{DD}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7V_{DD}$	-	-	-
$V_{hys(NRST)}$	NRST input voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	7	8	9	kΩ
$V_{F(NRST)}$	Minimum required reset pulse width	-	20	-	-	μs

Figure 7-7 Recommended NRST pin protection



Caution 1: The external capacitor protects the device against parasitic resets.

Caution 2: The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 7-25 NRST pin characteristics. Otherwise the reset will not be taken into account by the device.

7.3.13 12-bit ADC characteristics

Unless otherwise stated, the test data given in the table below is based on the test environment indicated by *Table 7-4 General operating conditions*.

Table 7-26 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Analog supply voltage for ADC ON	-	1.65	-	5.5	V
$I_{DD(ADC)}$	Current consumption of the ADC	V_{DD} = 3.3V	-	1.5	-	mA
f_{ADC}	ADC clock frequency	-	-	24	-	MHz
f_S	Sampling rate	-	-	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 24MHz	-	-	800	kHz
V_{AIN}	Conversion voltage range	-	0	-	V_{DD}	V
R_{AIN}	Input impedance(direct connect/buffer)	-	-	-	100	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	9	-	pF
t_S	Sampling time	-	5	-	10	1 / f_{ADC}
t_{STAB}	Stabilization time	-	19			1 / f_{ADC}
t_{CONV}	Total conversion time (including sampling time)	-	24	-	29	1 / f_{ADC}

Table 7-27 Accuracy of ADC[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max. [2]	Unit
ET	Composite error	f_{ADC} = 24MHz, V_{DDA} = 1.65V ~ 5.5V, T_A = -40°C ~+105°C	-	±2.5	±3.0	LSB
EO	Offset error		-	±1.5	±2.4	
EG	Gain error		-	±2.2	±2.7	
DNL	Differential nonlinearity		-	±0.5	±1.0	
INL	Integral nonlinearity		-	±1.0	±3.0	
SINAD	Signal-to-noise ratio distortion		-	67	-	dB
SNR	Signal-to-noise ratio		-	66	-	
THD	Total harmonic distortion		-	-70	-	
ENOB	Significant digits	V_{ref} = V_{DDA}/ExRef 25KSPS@V_{DDA} = 1.65V~1.8V 100KSPS@V_{DDA} = 1.8V~2V 200KSPS@V_{DDA} = 2V~2.4V	-	10.1	-	bits
		V_{ref} = V_{DDA}/ExRef 500KSPS@V_{DDA} = 2.4V~2.7V 1MSPS@V_{DDA} = 2.7V~5.5V	-	10.8	-	
		V_{ref} = Internal 1.5V reference voltage 100KSPS@V_{DDA} = 1.8V~2V 200KSPS@V_{DDA} = 2V~5.5V	-	9.7	-	
		V_{ref} = Internal 2.5V reference voltage 200KSPS@V_{DDA} = 2.8V~5.5V	-	10.0	-	

Caution 1 : ADC DC accuracy values are measured after internal calibration;

Avoid injecting reverse current on any analogue input pin as this can degrade the accuracy of conversions performed on another analogue input, it is recommended to add a Schottky diode (between the pin and ground) to the analogue pin where the reverse current will probably be injected;

Better performance can be achieved over restricted V_{DDA}, frequency, and temperature ranges.

Caution 2 : Data based on characterization results, not tested in production.

7.3.14 Temperature sensor characteristics

Table 7-28 TS characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L	VSENSE linearity with temperature	-	±2	±5	°C
Avg_Slope	Average slope	2.66	2.69	2.72	mV / °C
V_{25}	Voltage at 25°C (±5°C)	0.77	0.79	0.8	V
t_{START}	TS internal temperature sensor follower settling time	-	-	45	μs
t_{S_temp}	ADC sampling time when reading the temperature	5	-	-	μs

7.3.15 Analog voltage comparator characteristics

Table 7-29 Comparator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max. [1]	Unit
V_{DD}	Analog supply volgate	-	1.65	-	5.5	V
V_{IN}	Comparator input volgate range	-	0	-	V_{DD}	V
t_{START}	Startup time	Ultra low speed	-	10	10	µs
		Low speed	-	1	2	
		Medium speed	-	0.5	1	
		High speed	-	0.1	0.25	
t_D	Delay Time	Ultra low speed	-	10	10	
		Low speed	-	1	2	
		Medium speed	-	0.5	1	
		High speed	-	0.2	0.5	
V_{offset}	Offset Error	-	-	±3	±10	mV
dThreshold/dt	Threshold voltage temperature coefficient	V_{DD} = 3.3V, -40°C < T_A <+105°C , V-=(n/64)×V_{ref}	-	40	80	ppm/°C
$I_{DD(VC)}$	Current consumption	Ultra low speed	-	0.2	0.3	µA
		Low speed	-	1	1.2	
		Medium speed	-	8	10	
		High speed	-	16	20	
V_{hys}	Comparator hysteresis	Nohysteresis (VCx_CR0.HYS=00)	-	0	-	mV
		Low hysteresis (VCx_CR0.HYS=01)	-	10	-	
		Medium hysteresis (VCx_CR0.HYS=10)	-	20	-	
		High hysteresis (VCx_CR0.HYS=11)	-	30	-	

Caution 1: Data based on characterization results, not production tested.

7.3.16 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to Section *7.3.11 I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 7-30 Timer characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{res(TIM)}$	Timer resolution	-	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 48MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency	-	-	-	f_{TIMCLK} / 2	MHz
t_{MAX_COUNT}	Maximum period	-	-	-	65536	t_{TIMCLK}

Table 7-31 IWDT min/max timeout period at 10 kHz (RC10K)

Prescaler divider	IWDT_CR.PRS	Min timeout period	Max timeout period	Unit
4	0	0.417	2560	ms
8	1	0.834	5120	
16	2	1.667	10240	
32	3	3.334	20480	
64	4	6.667	40960	
128	5	13.334	81920	
256	6	26.667	163840	
512	7	53.334	327680	

Table 7-32 WWDT min/max timeout period at 48 MHz (PCLK)

Prescaler divider	Control bit	Min timeout period	Max timeout period	Unit
4096	0	0.086	3.413	ms
8192	1	0.171	6.826	
16384	2	0.342	13.653	
32768	3	0.683	27.306	
65536	4	1.366	54.613	
131072	5	2.731	109.226	
262144	6	5.461	218.428	
524288	7	10.923	436.906	

7.3.17 Communication interfaces

I2C interface characteristics

- The I2C interface meets the I2C-bus specification and the user manual:
  - Standard-mode(Sm): with a bit rate up to 100kbit/s
  - Fast-mode (Fm): with a bit rate up to 400kbit/s
  - Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s
- The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (Refer to Reference manual).
- The SDA and SCL I/O requirements are met with the following restrictions:
  - The SDA and SCL I/O pins are not "true" open-drain,maximum input voltage limited by specification.

    When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present.

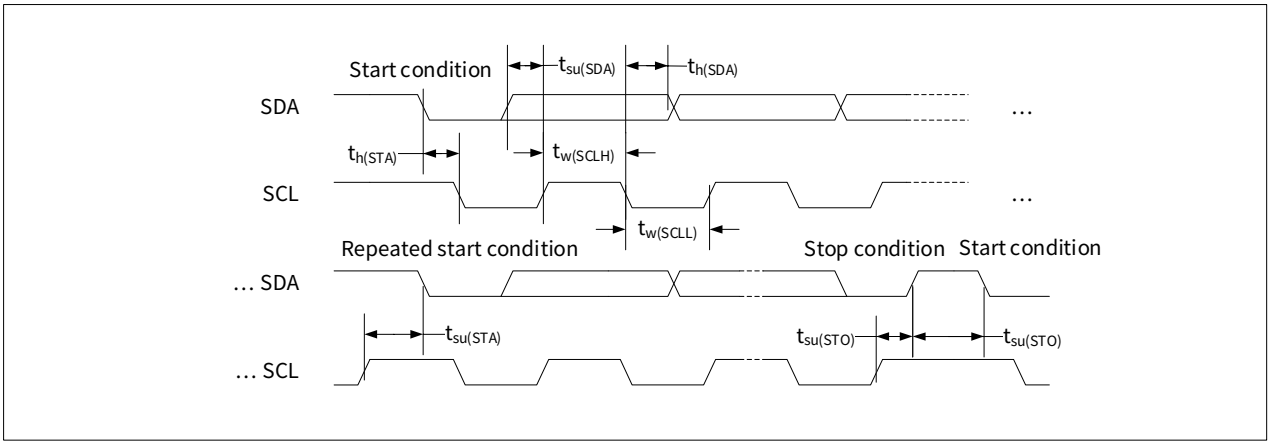
Refer to Section *7.3.11 I/O port characteristics* for the I2C I/Os characteristics.

Table 7-33 I2C characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.25	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	50	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{h(STA)}$	Start condition hold time	2.5	-	0.625	-	0.25	-	μs
$t_{su(STA)}$	Repeated start condition startup time	2.5	-	0.6	-	0.25	-	
$t_{su(STO)}$	Stop condition setup time	0.25	-	0.25	-	0.25	-	
$t_{w(STO:STA)}$	Stop condition to start condition time(Bus Idle)	4.7	-	1.3	-	0.5	-	

Caution 1: Guaranteed by design, not tested in production.

Figure 7-8 I2C timing diagram



SPI interface characteristic parameters

Table 7-34 SPI characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	10	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C=15pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4\times T_{PCLK}$	-	
$t_{h(NSS)}$	NSS hold time	Slave mode	$2\times T_{PCLK}+10$	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low setup time	Master mode, f_{PCLK}= 48MHz, SCK prescaler divider factor = 4	$T_{PCLK}-2$	$T_{PCLK}+2$	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode (SMP=1)	0	-	
		Slave mode	2	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	2	-	
		Slave mode	2	-	
$t_{v(SO)}$	Data output valid time	Slave mode f_{PCLK}= 48MHz	-	50	
$t_{v(MO)}$		Master mode	-	3	
$t_{h(SO)}$	Data output hold time	Slave mode f_{PCLK}= 48MHz	25	-	
$t_{h(MO)}$		Master mode	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode f_{PCLK}= 48MHz	45	55	%

Caution 1: Data based on characterization results, not tested in production.

Figure 7-9 SPI timing diagram - slave mode and CPHA=0

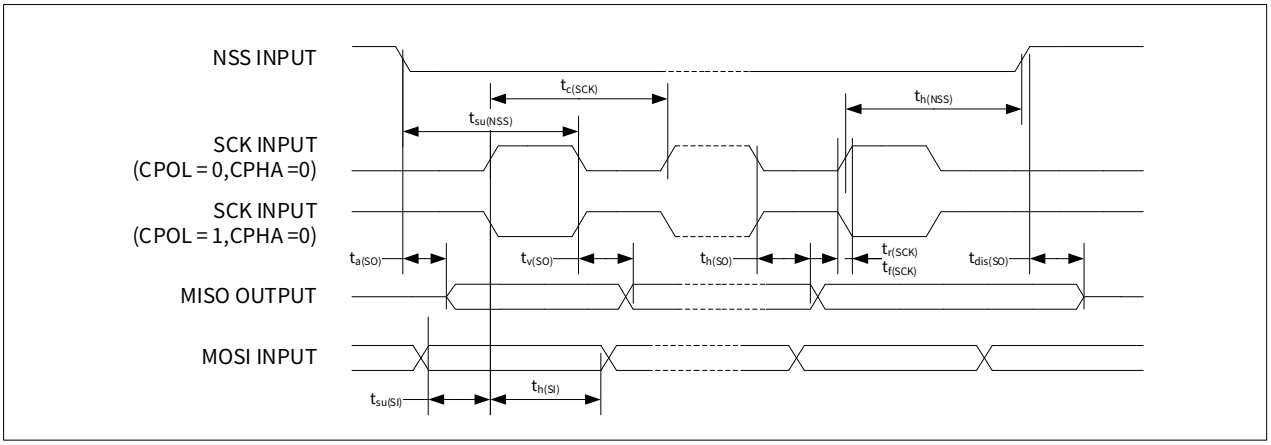


Figure 7-10 SPI timing diagram - slave mode and CPHA=1

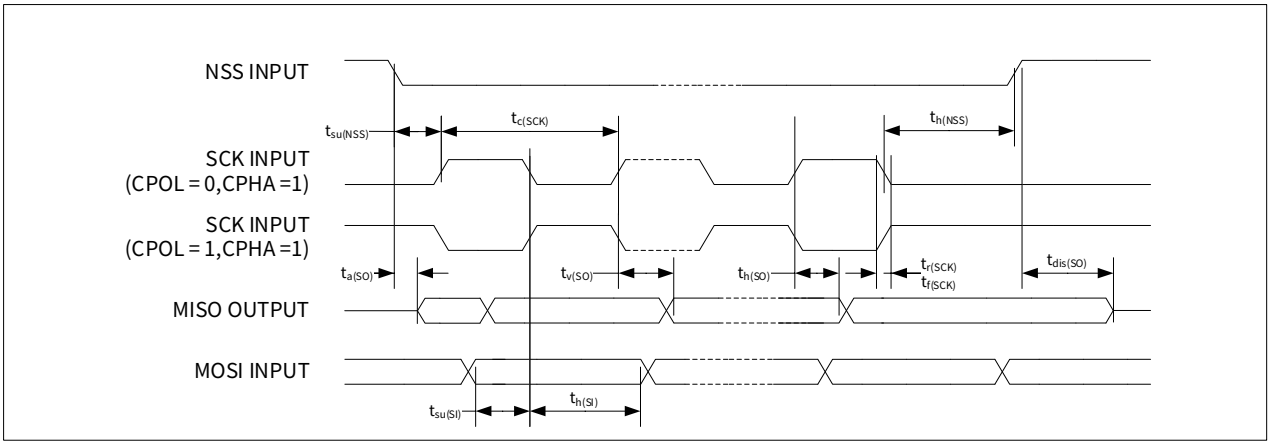
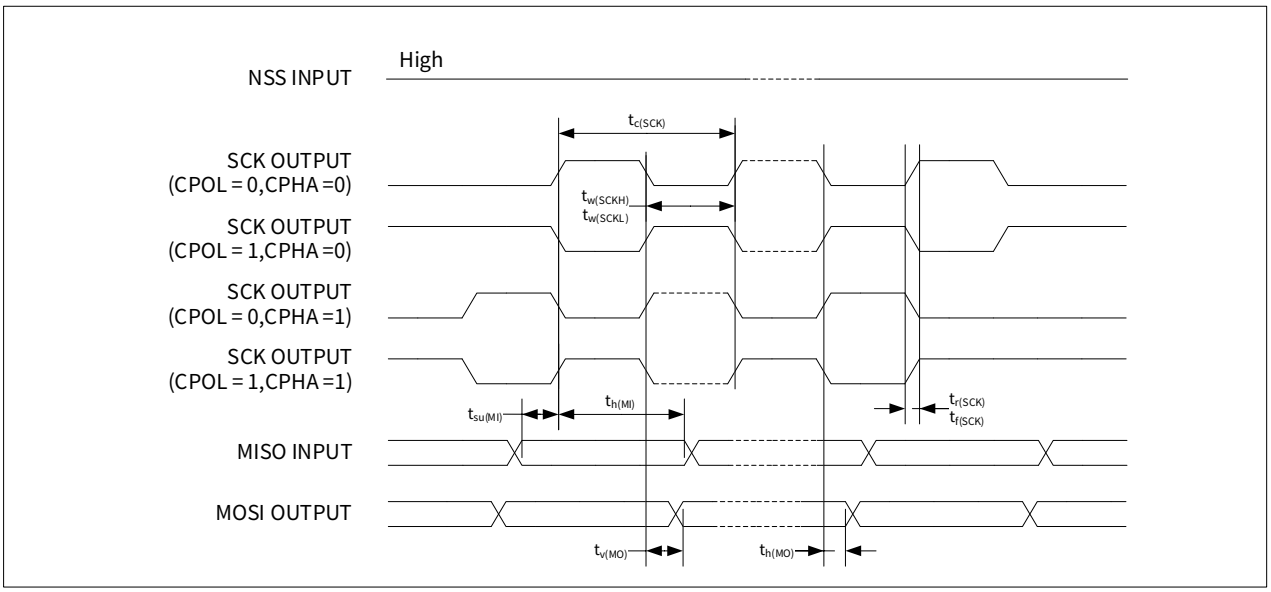


Figure 7-11 SPI timing diagram - master mode

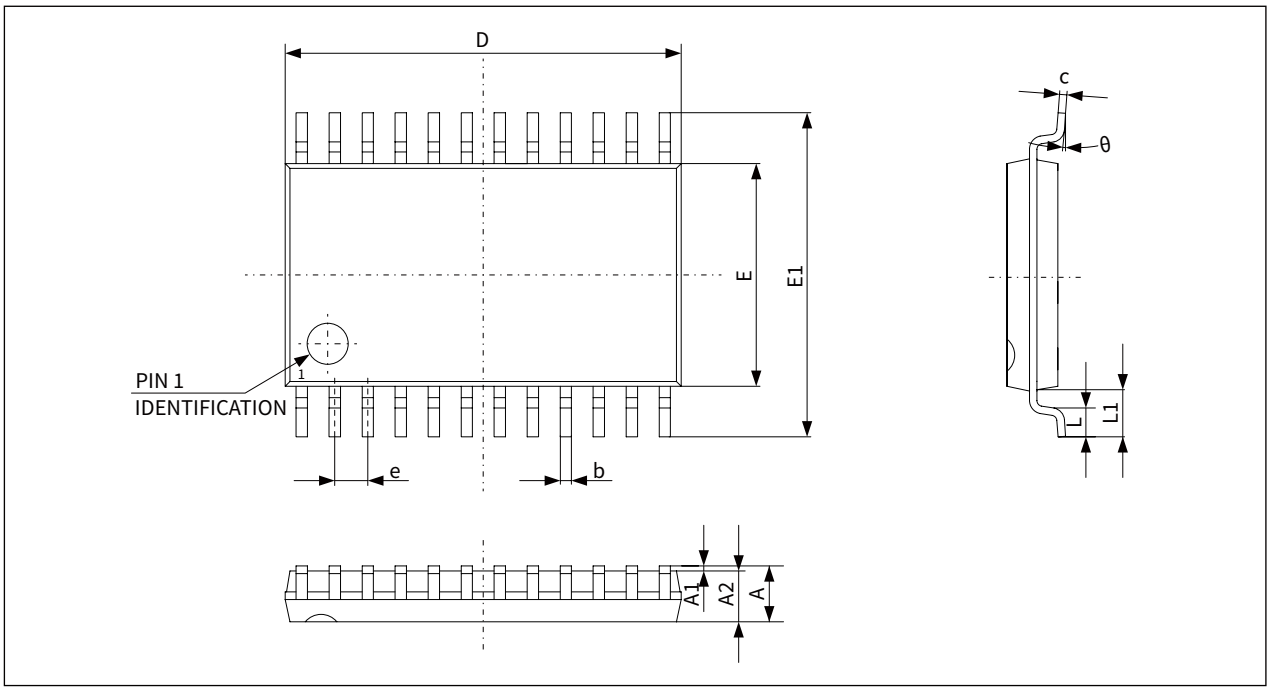


8 Package information

8.1 TSSOP24 package information

TSSOP24 is a 24-lead thin shrink small outline, 7.8 x 4.4mm, 0.65mm pitch package

Figure 8-1 TSSOP24 outline



Caution 1: Drawing is not to scale.

Table 8-1 TSSOP24 mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D	7.700	7.800	7.900	0.3031	0.3071	0.3110
E	4.300	4.400	4.500	0.1693	0.1732	0.1772
E1	6.800	6.400	6.600	0.2677	0.2520	0.2598
e	0.650BSC			0.0256BSC		
L1	1.000REF			0.0394REF		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
θ	0°	-	8°	0°	-	8°

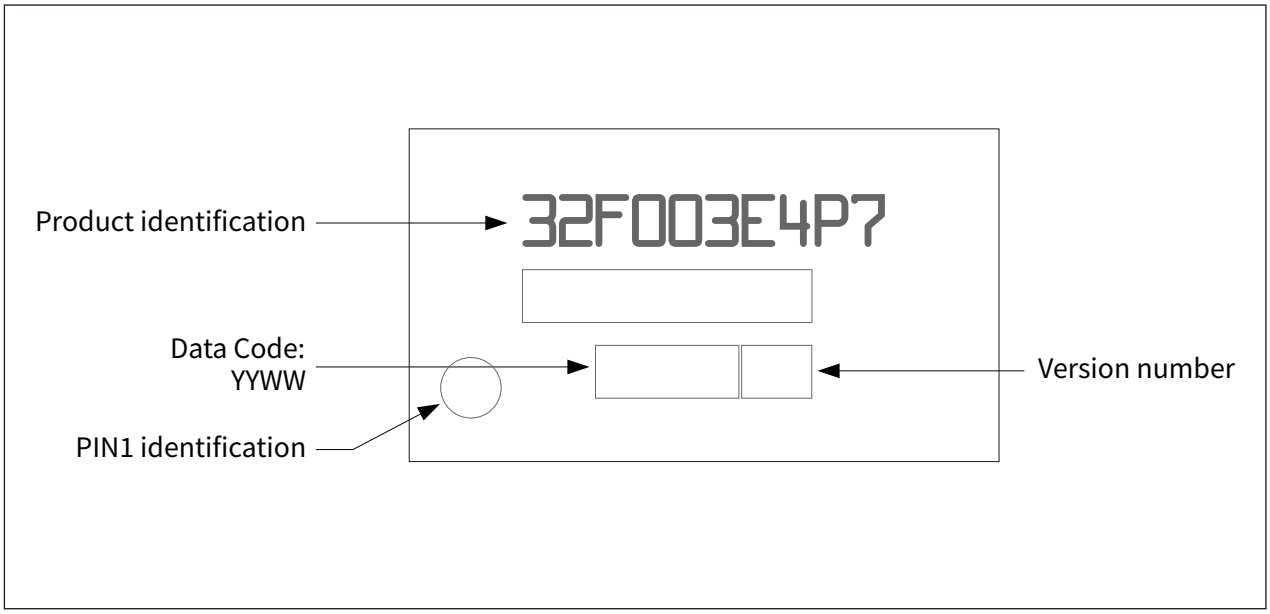
Caution 1: Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-2 TSSOP24 topside marking example

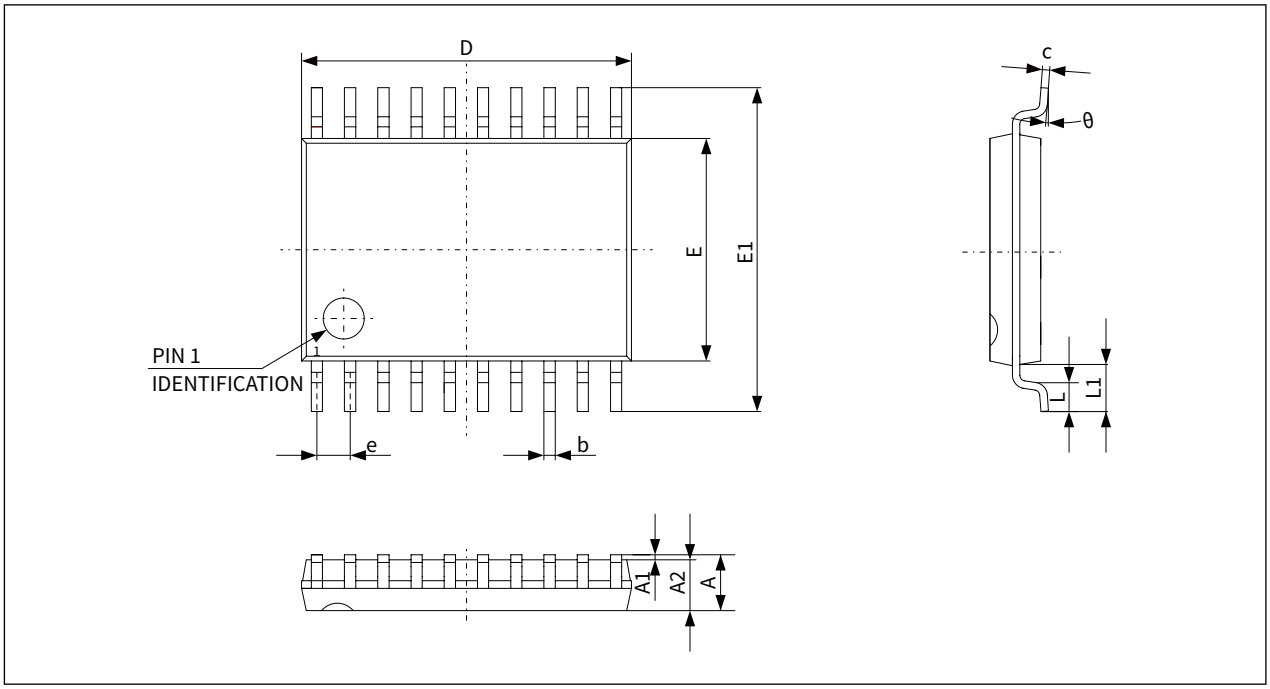


Caution 1: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.2 TSSOP20 package information

TSSOP20 is a 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch package.

Figure 8-3 TSSOP20 outline



Caution 1: Drawing is not to scale.

Table 8-2 TSSOP20 mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.900	1.000	1.050	0.0354	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	4.300	4.400	4.500	0.1693	0.1732	0.1772
E1	6.250	6.400	6.550	0.2461	0.2520	0.2579
e	0.650 BSC			0.0256		
L1	1.000 REF			0.0394		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
k	0°	-	8°	0°	-	8°

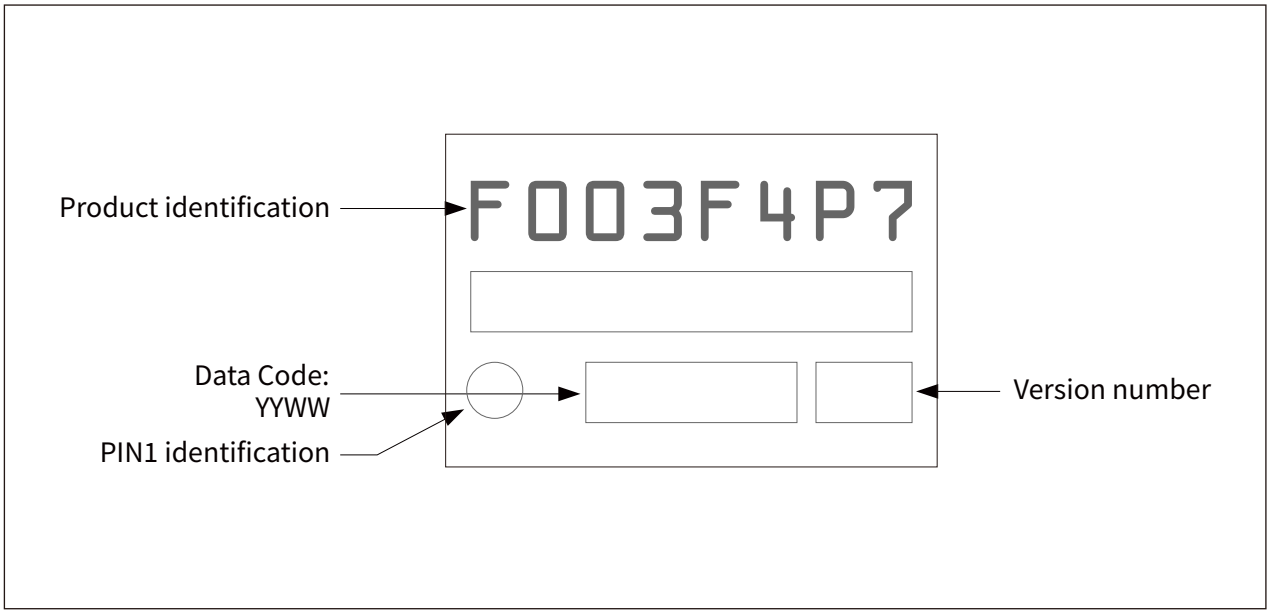
Caution 1: Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-4 TSSOP20 topside marking example

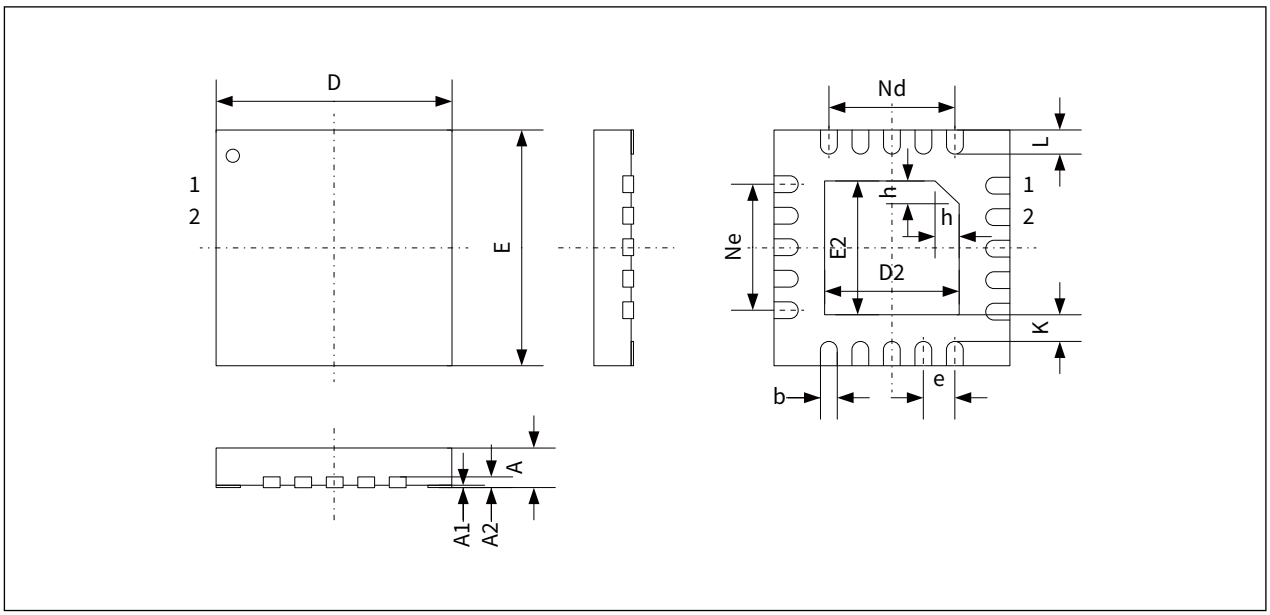


Caution 1: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.3 QFN20 package information

QFN20 is a 20-pin, 3.0 x3.0mm quad flat no-leads package.

Figure 8-5 QFN20 outline



Caution 1: Drawing is not to scale.

Table 8-3 QFN20 mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.450	0.500	0.550	0.0177	0.0197	0.0217
A1	-	0.020	0.050	-	0.0008	0.0020
A2	0.127 REF			0.0050 REF		
b	0.150	0.200	0.250	0.0059	0.0079	0.0098
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
D2	1.600	1.700	1.800	0.0630	0.0669	0.0709
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
E2	1.600	1.700	1.800	0.0630	0.0669	0.0709
e	0.400 BSC			0.0157 BSC		
K	0.250	0.350	0.450	0.0098	0.0138	0.0177
L	0.300	0.350	0.400	0.0118	0.0138	0.0157
h	0.250	0.300	0.350	0.0098	0.0118	0.0138
Ne	1.600 BSC			0.0630 BSC		
Nd	1.600 BSC			0.0630 BSC		

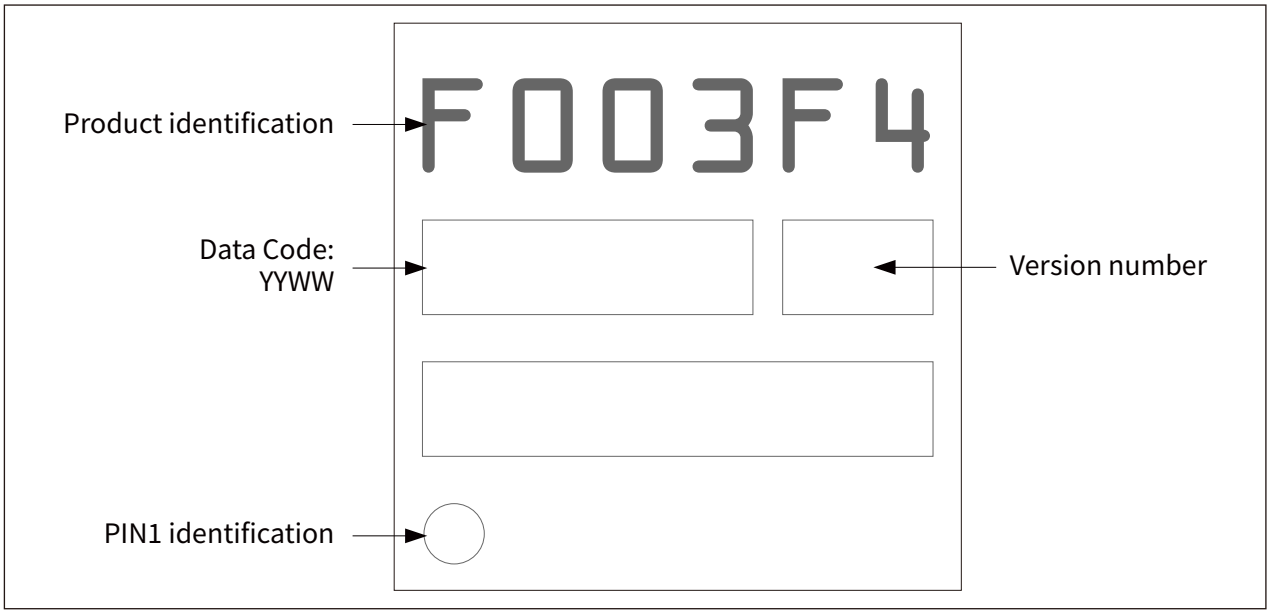
Caution 1: Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 8-6 QFN20 topside marking example



Caution 1: Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. CW is not responsible for any consequences resulting from such use. In no event will CW be liable for the customer using any of these engineering samples in production. CW's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.4 Thermal characteristics

The maximum chip junction temperature $T_J$max must never exceed the values given in *Table 7-3 Thermal characteristics*.

The maximum chip-junction temperature, $T_J$max, in degrees Celsius, may be calculated using the following equation:

$$T_J\ max = T_A max + (P_D max \times \Theta_{JA})$$

Where:

- $T_A$max is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C /W
- $P_D$max is the sum of P_{INT}max and $P_{I/O}$max ($P_D max = P_{INT} max + P_{I/O} max$)
- P_{INT}max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power
- $P_{I/O}$max represents the maximum power dissipation on output pins, where:

  $$P_{I/O} max = \Sigma\ (V_{OL} \times I_{OL}) + \Sigma\ ((V_{DD} - V_{OH}) \times I_{OH})$$

  The actual level and current conditions of the I/Os need to be included in the accurate calculation.

Table 8-4 Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20 – 6.5mm X 6.4mm	76	°C /W
	Thermal resistance junction-ambient QFN20 – 3.0mm X 3.0mm	90	

8.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from *www.jedec.org*

9 Ordering information

Example: CW32F003E4P7x

Device family
CW32=ARM-based

Product type
F=General-purpose

Sub-family
003=CW32F003xx

PIN count
F=20 pins
E=24 pins
K=32 pins

Code size
3=16 Kbytes Flash
4=20 Kbytes Flash

Package
P=TSSOP
U/V=QFN

Temperature range
6=-40°C~85°C
7=-40°C~105°C

Option
xxx=Programmed part
TR=tape and reel

Table 9-1 Minimum Order Quantity (MOQ)

MCU	Packaging	Quantity	MOQ	MSL	Note
CW32F003E4P7	Tube	60 pcs/Tube	8400 pcs	3	20 tubes/bundle, 7 bundles/box, 4 boxes/carton, single box vacuumized
CW32F003F4P7	Tube	70 pcs/Tube	9800 pcs	3	20 tubes/bundle, 7 bundles/box, 4 boxes/carton, single box vacuumized
CW32F003F4P7TR	Reel	4000 pcs/reel	4000 pcs	3	2 reels/box, 6 boxes/carton, single reel vacuumized
CW32F003F4U7	Reel	3000 pcs/reel	3000 pcs	3	10 reels/box, 4 boxes/carton, single reel vacuumized

10 Revision history

Table 10-1 Document revision history

Date	Revision	Changes
August 31, 2022	Rev 1.0	Initial release.